CHAPTER 2

TEST, ADJUSTMENT, CALIBRATION, FAULT FINDING and REPAIR

Table of Contents

Note:

In this chapter, screen "division" refers to the squares or boxes, i.e. five small divisions.

2.0 Introduction

This chapter is intended primarily for those who may have to test, modify, upgrade or repair a 9400 in the field, i.e. without the specialized test gear which is available at the large LeCroy offices. It will be assumed that the reader only has the normal electronic workshop facilities, but he should have the use of the following:

- Tektronix 485 analog scope or other fast scope
- Good FET probe for the above
- Function generator
- EHT dummy load or safe receptacle for an EHT cable

Because of the complex nature of the 9400 the provision of an exhaustive diagnostic system is not feasible: what is provided here is an attempt to give enough guidance to locate a fault to the correct board, and perhaps to pin-point the fault in easy cases. The arrangement of the boards within the 9400 <5.0.2> means that access to parts of the 9400-2 and 9400-3 boards is impossible, as is access to any part of the 9400-4. The two 9400-3 boards can, of course, be interchanged for test purposes, but should generally be replaced afterwards.

To make best use of this chapter, reference to the appropriate section of Chapter 1, the functional description, may be needed.

The usefulness of this chapter could be increased as more 9400s are delivered, if anyone who has useful ideas will send them to LeCroy SA or LeCroy Corporation for forwarding. Although in principle the standard repair report is a source of data on faults, it does not normally carry many details of procedures.

BASIC PERFORMANCE TEST PROCEDURE

2.1 Introduction

This chapter describes 9400 tests which require the use of LeCroy software. The 9400 software includes a small number of test routines which can be controlled from the front panel - these are described in Section 2. Because the system is easy to use, only a few of the operations are described in detail in this section.

Note

The following sections apply only to versions V2.0 and higher. If your Model 9400 has an earlier software version (check on the upper right-hand corner of the "Memory STATUS" display page), please ask your LeCroy contact for an update of your oscilloscope's software.

For further information on the comprehensive software package CALSOFT (order code CS01, CS02) for 9400 adjustment and calibration, refer to the CALSOFT operator's manual.

2.1.1 Turn-on

1. Check that the correct line voltage is set on the rear-panel power connector.

2. Check the following:

   a) that the display comes on after about 10 sec.

   b) that the display is stable (if traces are displayed, turn them all off).

   c) that the range of INTENSITY and GRID INTENSITY is reasonable.

3. Wait about 10 minutes for the 9400 to reach a stable temperature.

2.1.2 Test for Low Frequency Noise on the Input

This test verifies that the front-end components, ADC and power supplies operate correctly. Low frequency noise may be observed if any of the power supplies oscillate.

1. Turn on the Channel 1 and 2 traces, turn the others off.

2. Set the 9400 so that a single grid is displayed on the screen.

3. Set the controls of the 9400 as follows:

   a) Input coupling: 1 MΩ, DC (Channels 1 and 2)
   b) Fixed gain: 5 mV/div (Channels 1 and 2)
   c) Variable gain: 1 (Channels 1 and 2)

   d) Trigger - Slope: pos. or neg.
   Source: LINE
   Coupling: DC
   Mode: NORM
   Delay: zero

4. Setting the time base to 10, 5, 2, 1, and 0.5 msec/div in turn, check:

   a) that the displayed waveforms are constant bands less than 2/5 of a vertical division wide.
   b) that there is no discernible periodic structure.

5. Using the offset control, move the Channel 1 and Channel 2 traces slowly through the entire range and check that there is no change in the displayed trace. This is best seen by displaying only one trace at a time.

Solution to Problems

If there is a low frequency structure of the order of 1 kHz, check the following:

a) Is the lower RF-shield of the front-end correctly installed? In some of the older versions, the screw head which holds the right-hand front foot of the lower 9400 cover may push the RF-shield towards the 9400-1 main board, creating shorts circuits. Verify that the absence of the lower 9400 cover has no effect on the noise problem.

b) Have any of the 4 supply voltages oscillations of more than 50 mV (peak-to-peak) amplitude in the frequency range of 50 Hz to 200 kHz (check for time-base settings 10 msec/div through 10 µsec/div). If this is the case, the power supply must be repaired. Note that power supply oscillations may occur particularly at high temperatures (use a heat gun to verify a repair).

2.1.3 Offset

1. Set up the 9400 as follows:

   a) Channel 1: on (turn off all the others)
   b) Volts/div: 5 mV/div
   c) Time base: 10 msec/div

   d) Trigger - Mode: Norm
   - Source: line
   - Slope: Pos. or neg.
   - Input set to GND

2. Switch the bandwidth limit on and then off again to calibrate both channels.

3. Center the trace in the middle of the screen.

4. Switching between a) 1 MΩ: DC and GND,
   b) 50 Ω: DC and GND,
   c) 50 Ω: AC input and GND,

   check that the trace does not vary more than 1 minor division, approximately 1 mV.

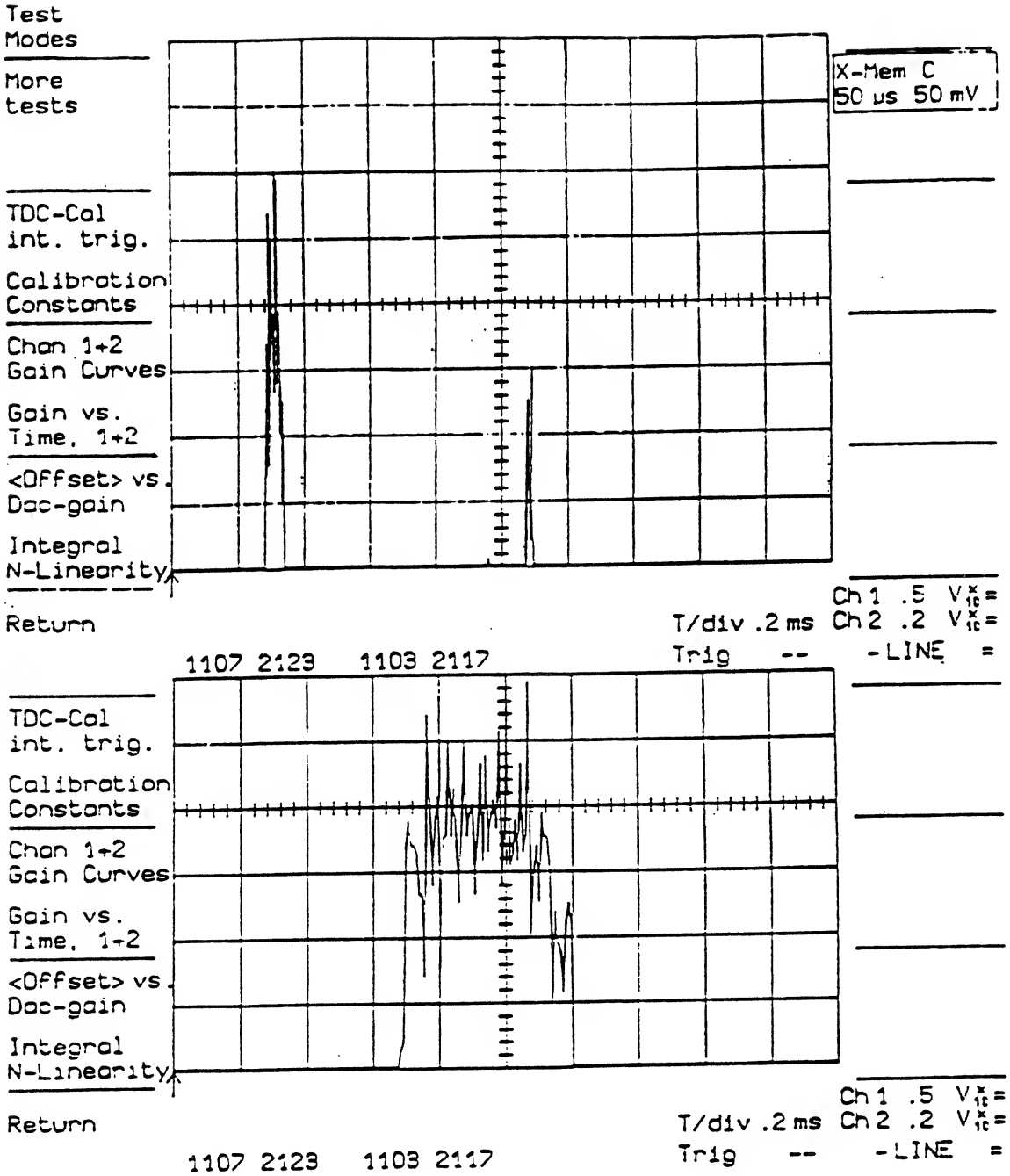
5. Repeat steps 1 through 4 with Channel 2 on and Channel 1 off.

6. If any channel fails the offset test, measure the input impedance in the 1 MΩ and 50.5 Ω DC modes with an ohmmeter. The readings should be within 1%.

2.1.4 Front-end Check

1. Set up the 9400 as follows:

   a) Channel 1 on, (all other traces off)
   b) Trigger - Source: Ch 1,
   - Coupling: DC coupling
   - Mode: norm
   - Delay: 0
   - trigger level: 0.00 div.
   - Slope: negative or positive



INITIAL AND EXPANDED TDC TEST WAVEFORM

Figure 1

2.1.8 Gain Curves

This test allows the user to check whether the dynamic range of the programmable input amplifiers is sufficient. If it is not, the 9400 cannot calibrate itself correctly, and the ground line jumps when the bandwidth limit is switch on and off.

1. Set the bandwidth limit OFF.

2. Set the Channels 1 and 2 VOLTS/DIV controls to 5 mV/div.

3. Push the soft key "Chan 1 and 2 Gain Curves". The gain curves should appear within 5 seconds.

4. Check that the 2 gain curves (shown in Figure 2):

   a) are at least 1/4 division above the gain = 1 line on the left flat-top.

   b) decrease to at least 1/4 division below the gain = 0.4 line.

5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:
   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF

c) Channel 1: Volts/div: 1 V/div,
Time base: 0.1 µsec/div.
Signal coupling: 50 Ω

2. Connect a 6 V p-p 1 MHz square wave from a function generator (50 Ω output) to CH 1.

3. Set the interleaved sampling mode on.

4. Check the following:

   - On the rising and falling edges there should not be a large (e.g. + 20%) overshoot.

5. Repeat step 4 using a 600 mV p-p signal with Channel 1 Volts/div set to 0.1 V/div.

6. Repeat step 4 using a 60 mV p-p signal with Channel 1 Volts/div set to 10 mV/div.

7. Repeat steps 1 through 6 for CH 2 (trigger source CH 2).

8. When both channels have been checked at 50 Ω, use an in-line 50 Ω terminator and set the 9400 to 1 MΩ input, DC coupling. Repeat steps 1 to 7 for both channels using these new settings.

2.1.5 Preparation for Internal Tests

The 9400 is capable of executing a number of autonomous tests, the results of which are stored in reference memory C, and normally accessed through the (expanded) display controls. Whenever the test menu is entered (see Section 7), the entire Memory C buffer is cleared and the 9400 is set to display the expansion of Memory C under trace "EXPAND A". When each individual test is performed, the 9400 automatically expands the display and centers it on the newly acquired histogram. You may nevertheless use the manual controls of "EXPAND A" to further modify the display, if required.

2.1.6 Entering the Internal Test Menu

1. Ensure that the 9400 is in the "root" menu, i.e. only "Main Menu" should appear to the left of the grid. Otherwise push the "Return" button until this is the case.

2. While keeping the lowest menu button (the one above SCREEN DUMP) pressed, push the top button, "Main Menu". The "Test Modes" menu should appear.

3. To make sure that the 9400 triggers, set the trigger controls as follows:

   Trigger source: LINE
   Trigger mode: NORM

This ensures that the front-end is recalibrated whenever the input conditions are modified during the following test procedures.

2.1.7 Internal TDC Calibration

The 9400 calibrates the 10 psec time interpolator on the 100 MHz time base when the time base is modified. If this calibration fails (i.e. one of the peaks described below is missing), this may give rise to "jumps" in the display of INTERLEAVED waveforms at intervals of 10 nsec.

1. Push the fourth soft key "TDC-Cal, int. trig.". Within less than a second, the distribution displayed in the upper screen picture in Figure 1 should appear.

2. Check that the distribution contains 2 peaks, each at least 2 vertical divisions high.

3. Use the Position knob to center the left-hand peak on the display.

4. Turn the Time Magnifier knob clockwise to expand to 5 µsec/div.

5. Check that the width of the distribution is more than 1 horizontal division.

6. Repeat steps 3, 4 and 5 for the right-hand peak.

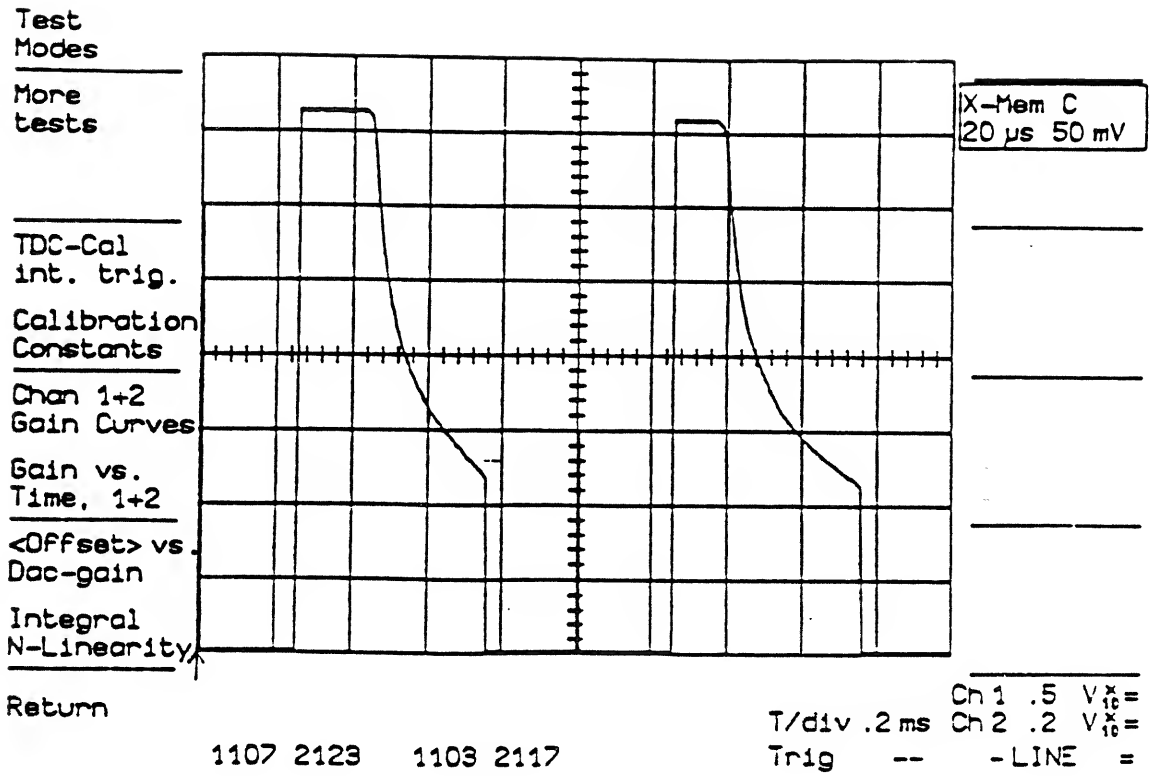
Solution to Problems

If either peak is missing or is too narrow, adjust the timing capacitor (TEST DLY ADJ) on the 9400-4 time-base card as follows:

1. Remove the top cover.

2. Locate the capacitor which is about 2 inches below the rear edge of the 9400-8 timing bus card.

3. Turn the capacitor 1/8 of a turn either way and check its effect by redoing the measurement, i.e. by pushing "TDC-Cal, int. trig."



GAIN CURVES

Figure 2

2.1.9 Gain vs. Time

This test permits the user to verify that the 9400 reliably measures the gain of the front-end amplifiers. It may not do so if there is noise present which influences the gain measurement. In this case, the calibration of the front-end may not work.

Note: this test is performed with the calibrated gain set to 1.00. The vertical scale is changed to 1 percent per division for easier observation. The absolute position of the measured gain is a measure of the precision of the gain calibration.

1. Set the Bandwidth Limit OFF.

2. Set the VOLTS/DIV control of Channels 1 and 2 to 5 mV/div.

3. Press the soft key "Gain vs. Time, 1 + 2". The new distributions should appear within 15 seconds.

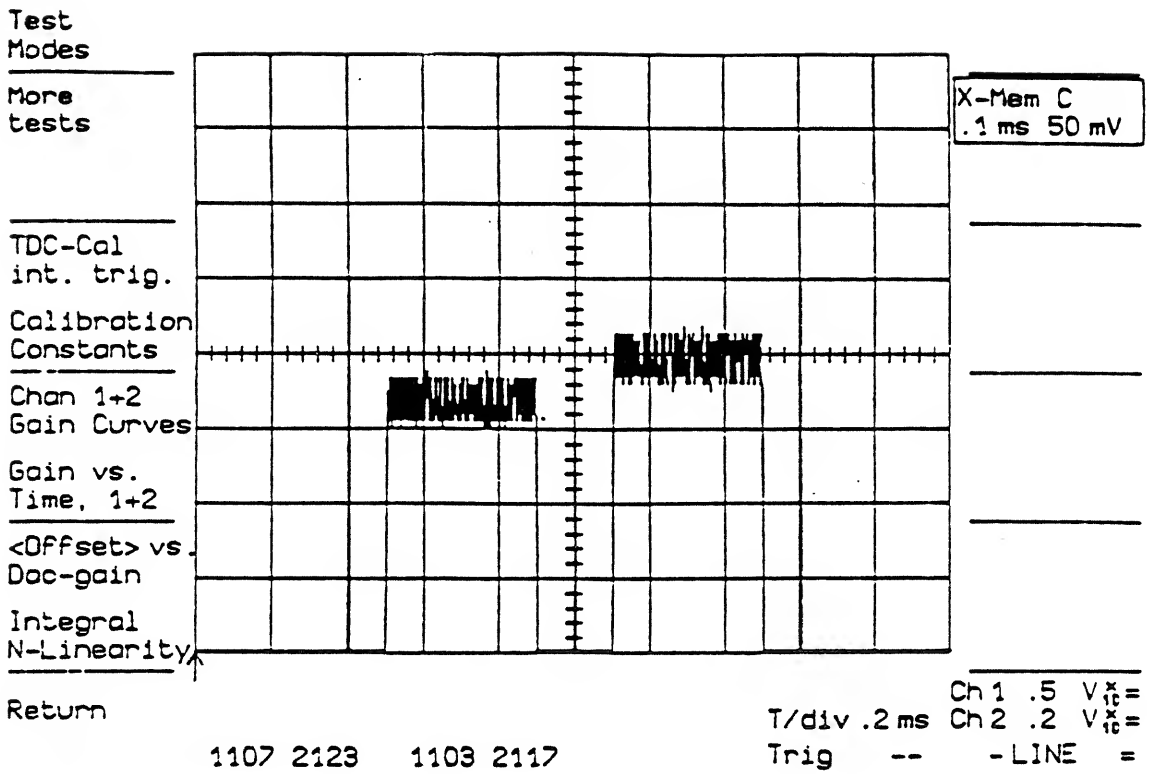
4. Check the two curves (which should resemble those shown in Figure 3) as follows:
   The deviation from the center (1.0 gain) line should be within the following limits.

Gain	1% DSO	2% DSO
5 mV/div	± 1.5%	± 2%
other	± 0.8%	± 1.5%

5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:
   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF.
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF.

Solution to Problems

If the width of the band is too large, check for low-frequency noise, (see Section 3).



GAIN VS. TIME CURVES

Figure 3

2.1.10 <Offset> vs. Gain-DAC

This test permits the user to check if the offset of the second front-end amplifier has been correctly adjusted.

1. Set the Bandwidth Limit OFF.

2. Set the VOLTS/DIV control of Channels 1 and 2 to 5 mV/div.

3. Press the menu button "<Offset> vs. Dac-gain". The new curves should appear within 20 seconds.

4. Check the two offset curves (as shown in Figure 4)

   a) the curves should be rather horizontal, i.e. the difference between the left edge and the right edge should be less than 1 vertical division.

   b) the vertical position of the curve should lie in the 4 major central divisions.

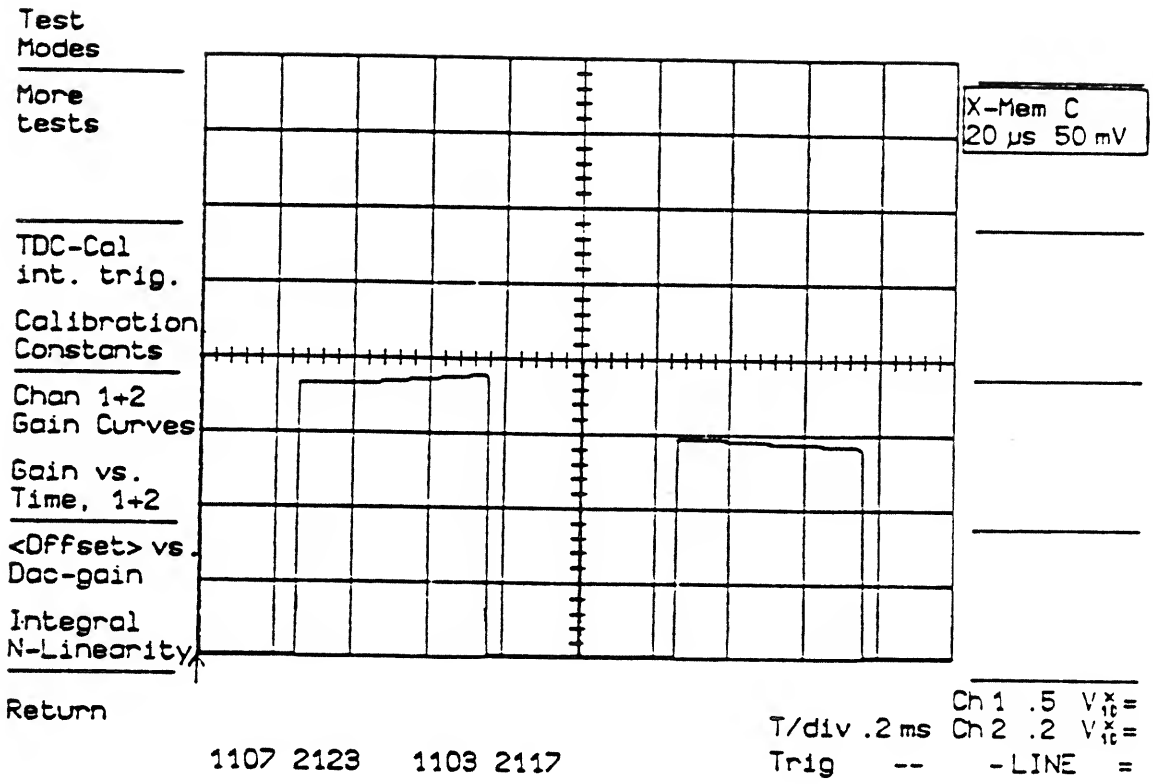
5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:

   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF.
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF.

NOTE: Since the adjustment of the output offset of the HVV200 is common to bandwidth limit ON and OFF, check that the deviations from a horizontal curve are as symmetrical as possible, i.e. by equal amounts above and below the center.

Solution to Problems

If an offset curve is not horizontal enough, the offset of the second amplifier (within the HVV200) must be readjusted. This requires a repetition of the calibration of the output offset of the corresponding HVV200.



OFFSET VS. GAIN DAC

Figure 4

2.1.11 Integral Non-Linearity

This test allows the user to check the DC integral non-linearity and the offset-calibration of the front-end amplifiers.

1. Set the Bandwidth Limit OFF.
2. Set the VOLTS/DIV control of channels 1 and 2 to 5 mV/div.
3. Press the soft key "Integral N-Linearity". The new curves should appear within about 10 seconds.
4. Check the integral non-linearity curves. (Figure 5 shows an example where the results for channel 1 are not satisfactory.)

   The curves must be within the following deviation from the center (0%) line. (1 division = 1%.)

Curve	0 (leftmost)	1	2	3	4 (rightmost)
Gain					
5 mV/div	2.5%	2%	2%	2%	2.5%
other	2%	2%	1.5%	2%	2%

5. Repeat the test described above in steps 3 and 4 with the following settings of the 9400:

   a) Ch. 1 and 2: 5 mV/div; bandwidth limit ON.
   b) Ch. 1 and 2: 10 mV/div; bandwidth limit ON and OFF.
   c) Ch. 1 and 2: 20 mV/div; bandwidth limit ON and OFF.
   d) Ch. 1 and 2: 50 mV/div; bandwidth limit ON and OFF.

Solution to Problems

If any of the curves is outside the limits, the HVV200 of the corresponding channel has an integral non-linearity out of specification and should be exchanged. However, a bad offset calibration may give rise to deviations outside this tolerance. This would show up as a systematic vertical offset of the outermost curves (of the 5 sub-curves) with respect to the other curves.

6. Read the frequency of the SG 503. The bandwidth specification for the 3 dB point is as follows:

	9400 [MHz]	9400A [MHz]
5 mV/div	125	150
1 V/div	140	225
Other	140	175

7. Connecting the output of the SG 503 to Channel 1 or 2 as required, repeat steps 4 to 6 for the following settings of the 9400.

   a) Channel 2, 1 V/div
   b) Channel 1 and 2, 0.5 V/div
   c) Channel 1 and 2, 0.2 V/div
   d) Channel 1 and 2, 0.1 V/div
   e) Channel 1 and 2, 50 mV/div
   f) Channel 1 and 2, 20 mV/div
   g) Channel 1 and 2, 10 mV/div
   h) Channel 1 and 2, 5 mV/div

8. Repeat steps 1 to 7 with the bandwidth limiter ON. The 3 dB point should now be at 30 MHz ± 20%.

2.1.13 Bandwidth Test at 1 MΩ Input Impedance

The purpose of this test is to ensure that the entire 9400 system has a bandwidth within specification at 1 MΩ input impedance.

1. Set up a Tektronix SG 503 Leveled Sine Wave Generator or equivalent instrument as follows:

   a) Frequency: approximately 0.5 MHz
   b) Amplitude Multiplier: × 1
   c) Output Amplitude 5.0

2. Connect the output of the SG 503 to the Channel 1 input of the 9400 through a 50 Ω feed-through terminator.

3. Set the 9400 as follows:

   a) Channel 1 trace: On (turn off all other traces)

   b) Trigger: Slope: pos. or neg.
   Source: CHAN 1
   Coupling: DC
   Mode: NORM
   Delay: ZERO
   Level: 0.00 div

   c) Channel 1 input: Signal coupling: 1 MΩ
   Gain: 1 V/div
   Var. Gain: 1
   Offset: about 0

   d) Time base: 0.5 µsec/div

   e) Interleaved sampling: ON

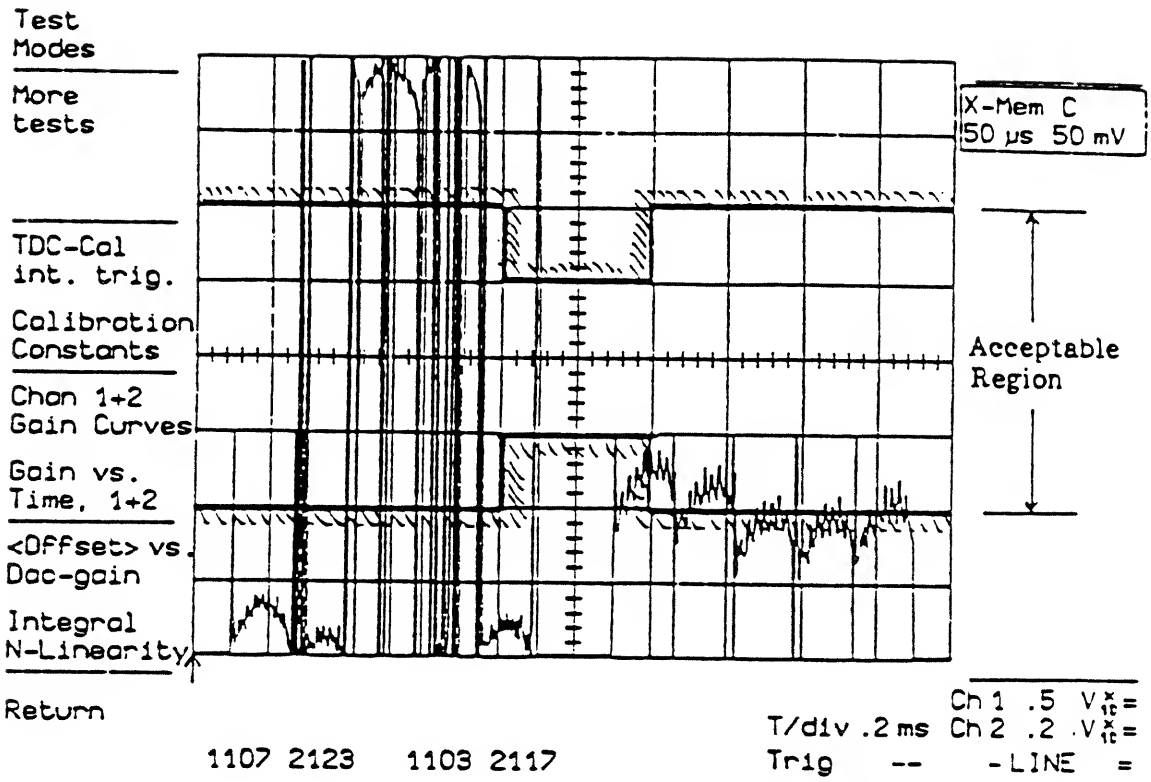
   f) Bandwidth Limit: OFF

4. Adjust the SG 503 Output Amplitude and Channel 1 offset to get a 5 division peak-to-peak sine wave.

5. Increase the SG 503 frequency while decreasing the Time/div until the sine wave peak-to-peak amplitude is 0.7 x 5 divisions = 3.5 divisions (3 dB point).

6. Read the frequency of the SG 503. The bandwidth specification for the 3 dB point is as follows:

	9400 [MHz]	**9400A [MHz]**
≥ 1 mV/div	80	80
Other	85	90



INTEGRAL NON-LINEARITY CURVES

Figure 5

2.1.12 Bandwidth Test at 50 Ω Input Impedance

The purpose of this test is ensure that the entire 9400 system has a bandwidth within specification at 50 Ω input impedance.

1. Set up a Tektronix SG 503 Leveled Sine Wave Generator or equivalent instrument as follows:

    a) Frequency: approximately 0.5 MHz
    b) Amplitude Multiplier: x 1
    c) Output Amplitude 5.0

2. Connect the output of the SG 503 to the Channel 1 input of 9400

3. Set the 9400 as follows:

    a) Channel 1 trace: On (turn off all other traces)

    b) Trigger: Slope: pos. or neg.
    Source: CHAN 1
    Coupling: DC
    Mode: NORM
    Delay: ZERO
    Level: 0.00 div

    c) Channel 1 input: Signal coupling: 50 Ω
    Gain: 1 V/div
    Var. Gain: 1
    Offset: about 0

    d) Time base: 0.5 µsec/div

    e) Interleaved sampling: ON

    f) Bandwidth Limit: OFF

4. Adjust the SG 503 Output Amplitude and Channel 1 offset to get a 5 division peak-to-peak sine wave.

5. Increase the SG 503 frequency while decreasing the Time/div until the sine wave peak-to-peak amplitude is 0.7 x 5 divisions = 3.5 divisions (3 dB point).

7. Connecting the output of the SG 503 to Channel 1 or 2 as required, repeat steps 4 to 6 for the following settings of the 9400.

   a) Channel 2, 1 V/div
   b) Channel 1 and 2, 0.5 V/div
   c) Channel 1 and 2, 0.2 V/div
   d) Channel 1 and 2, 0.1 V/div
   e) Channel 1 and 2, 50 mV/div
   f) Channel 1 and 2, 20 mV/div
   g) Channel 1 and 2, 10 mV/div
   h) Channel 1 and 2, 5 mV/div

8. Repeat steps 1 to 7 with the bandwidth limiter ON. The 3 dB point should now be at 30 MHz ± 20%.

2.1.14 Trigger Level Test for DC and HF REJ

1. Set up any sine wave generator capable of generating sine waves up to 100 Hz frequency, e.g. an Intron IFG-422 or TFG-8101, as follows:

   Frequency: approximately 100 Hz

2. Connect the output of the generator to the EXTERNAL input of the 9400 and to the Channel 1 input, using a coaxial T-connector (no 50 Ω feed-through terminator). The cable length between EXTERNAL and CHAN 1 should be chosen so that the propagation delay is not greater than 2 nsec.

3. Set the controls of the 9400 as follows:

   a) Full Grid

   b) Turn off all traces, except Channel 1

   c) Time base: 1 msec/div

   d) Channel 1 input: Signal coupling: 1 MΩ, DC
      Gain: 0.5 V/div
      Var. Gain: 1
      Offset: 0

   e) Trigger: Source: CHAN 1
      Mode: NORM
      Delay: 50% Pre-trigger (center of screen)
      Level: 0.00 div

4. Adjust the output amplitude of the sine wave generator to get an 8 division peak-to-peak sine wave, (corresponding to a 2 V amplitude). It is important that the offset of the input be set to zero (use the Panel STATUS menu to verify). Use the offset adjustment of the sine wave generator to center the signal in relation to the screen. Later, the test on the external trigger level requires that the signal should have an absolute range of ± 2 V.

5. Check the sine wave. It should pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position zero (vertical center) within ± 0.6 division.

6. Adjust the 9400 settings as listed first in (a) and then in (b) below. For each, check the resulting sine wave:

   It must pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position + 3 div (i.e. the second line from the top) within ± 0.6 division.

   a) Trigger Coupling: DC
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: + 3.00 div

   b) Trigger Coupling: HF REJ
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: + 3.00 div

7. Adjust the 9400 settings as listed first in (a) and then in (b) below. For each check the resulting sine wave.

   It must pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position - 3 div (i.e. the second line from the bottom) within ± 0.6 div.

   a) Trigger Coupling: DC
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: - 3.00 div

   b) Trigger Coupling: HF REJ
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: - 3.00 div

8. Disconnect the input from Channel 1 and connect it to input of Channel 2.

9. Turn off all traces, except Channel 2.

10. Set Input Channel 2: Coupling: 1 MΩ, DC
    Gain: 0.5 V/div
    Var. Gain: 1
    Offset: 0

11. Set Trigger Source to CHAN 2.

12. Repeat steps 4 through 7 for channel 2.

13. Leave the input connected to Channel 2 and leave Channel 2 on.

14. Set Trigger Source to EXT.

15. With the trigger level set first to + 1.5 V and then - 1.5 V, repeat steps 4 through 7 for the EXTERNAL trigger. Observe the effect on channel 2. Tolerance for the checkpoints: ± 0.8 div.

2.1.15 Trigger Level Test for AC and LF REJ

1. Set any sine wave generator capable of generating sine waves up to 2 MHz frequency, e.g. an Intron IFG-422 or TFG-8101 or Tektronix SG 503 LEVELED SINE WAVE GENERATOR, as follows:

   Frequency: approximately 2 MHz

2. Connect the output of the generator to the EXTERNAL input of the 9400 and to the Channel 1 input, using a coaxial T-connector. The cable length between EXTERNAL and CHAN 1 should be chosen so that the propagation delay is not greater than 2 nsec. If a Tektronix SG 503 is used, terminate at the Channel 1 input with a 50 Ω feed-through terminator.

3. Set the controls of the 9400 as follows:

   a) Turn off all traces except Channel 1.

   b) Time/div: 0.2 µsec/div.

   c) Interleaved sampling: OFF.

   d) Channel 1 input:

Signal coupling:	1 MΩ, DC
Gain:	0.5 V/div
Var. Gain:	1
Offset:	0

   e) Trigger:

Source:	CHAN 1
Mode:	NORM
Delay:	50 % Pre-trigger (center of screen)
Level:	0.00 V.

4. Adjust the output amplitude of the sine wave generator to get about an 8 division peak-to-peak sine wave, i.e. corresponding to a 2 V amplitude. It is important that the offset of the input be set to zero (use the Panel STATUS menu to verify this). Use the offset adjustment of the sine wave generator to center the signal with respect to the screen. Later, the test on the external trigger level requires that the signal have an absolute range of ± 2 V.

5. Check the sine wave. It must pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position zero (vertical center) within ± 0.6 division.

6. Adjust the 9400 settings as listed first in (a) and then in (b) below. For each, check the resulting sine wave:

   It must pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position + 3 div (i.e. the second line from the top) within ± 0.6 division.

   a) Trigger Coupling: AC
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: + 3.00 div

   b) Trigger Coupling: LF REJ
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: + 3.00 div

7. Adjust the 9400 settings as listed first in (a) and then in (b) below. For each check the resulting sine wave.

   It must pass through the horizontal center (50% pre-trigger line) of the screen at the vertical position - 3 div (i.e. the second line from the bottom) within ± 0.6 div.

   a) Trigger Coupling: AC
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: - 3.00 div

   b) Trigger Coupling: LF REJ
      Trigger Slope: POS and NEG (verify slope at check point)
      Trigger Level: - 3.00 div

8. Disconnect the input from Channel 1 and connect it to input of Channel 2.

9. Turn off all traces, except Channel 2.

10. Set Channel 2 input: Signal Coupling: 1 MΩ, DC
    Gain: 0.5 V/div
    Var. Gain: 1
    Offset: 0

11. Set Trigger Source to CHAN 2.

12. Repeat steps 4 though 7 for channel 2.

13. Leave the input connected to Channel 2 and leave the trace of Channel 2 on.

14. Set Trigger Source to EXT.

15. With the trigger level set to + 1.5 V and - 1.5 V, repeat steps 4 through 7 for the EXTERNAL trigger. Observe the effect on channel 2. Tolerance for the checkpoints: ± 0.8 div.

2.1.16 Bandwidth Test of the Trigger

This test checks the bandwidth of the trigger circuits.

1. Set up a Tektronix SG 503 LEVELED SINE WAVE GENERATOR as follows:

   a) Frequency: 200 MHz
   b) Amplitude Multiplier: X 1
   c) Output Amplitude: 5.5 (i.e. max.).

2. Connect the output of the SG 503 to the EXTERNAL input of the 9400 and also to the Channel 1 input using a coaxial T-connector. The cable length between EXTERNAL and CHAN 1 should be chosen so that the propagation delay is not greater than 2 nsec.

3. Set the controls of the 9400 as follows:

   a) Turn off all traces, except Channel 1.

   b) Time base: 5 nsec/div.

   c) Interleaved sampling: ON

   d) Channel 1: Coupling: 50 Ω, DC
      Gain: 0.5 V/div
      Var. Gain: 1
      Offset: 0

   e) Trigger: Source: EXT
      Mode: NORM
      Delay: 50% Pre-trigger (center of screen)
      Level: 0.00 V
      Coupling: DC, LF Rej and AC sequentially

4. The 9400 must keep triggering in a stable way (i.e. a strongly attenuated 200 MHz sine wave must be visible on the display) for all 3 couplings while the trigger level is at ± 0.20 V.

2.1.17 Manual time-base calibration with WWV standard signal (1 MHz)

Any 1 MHz sine wave generator with an accuracy better than 1 ppm can be used (for example a Marconi 2019A).

1. Press the following sequence of menu buttons:

   Main Menu
   Recall PANEL
   Default
   Menu Off.

2. Set the controls of the 9400 as follows:

   a) Channel 1: Signal coupling: 50 Ω DC
   Gain: 1 V

   b) Time base: 2 µsec/div

3. Select the main menu and press the button corresponding to the Panel Status Menu.

4. Adjust the **Vertical Offset** knob for channel 1 until 0.00 V is displayed.

5. Adjust the trigger settings as follows:

   Delay: 0% Pre- (Touch ZERO)
   Level: 00 Div
   Coupling: DC
   Source: CHAN 1
   Slope: +
   Mode: Normal

6. Ensure that the Panel Status Menu is as shown in Figure 6.

9400/A Time Base Verifcation

USE THIS PROCEDURE IN PLACE OF THE BASIC PERFORMANCE TEST STEP 18.

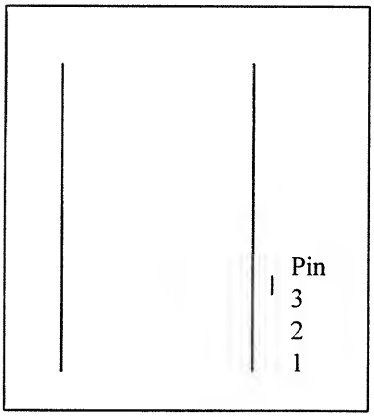
Check the frequency (50 or 100 MHz) from the TDC board on the 9400-8 clock bus board on line 2 or 3 from the front of the board, see fig. 1. **The Time Base accuracy is 0.002%.**

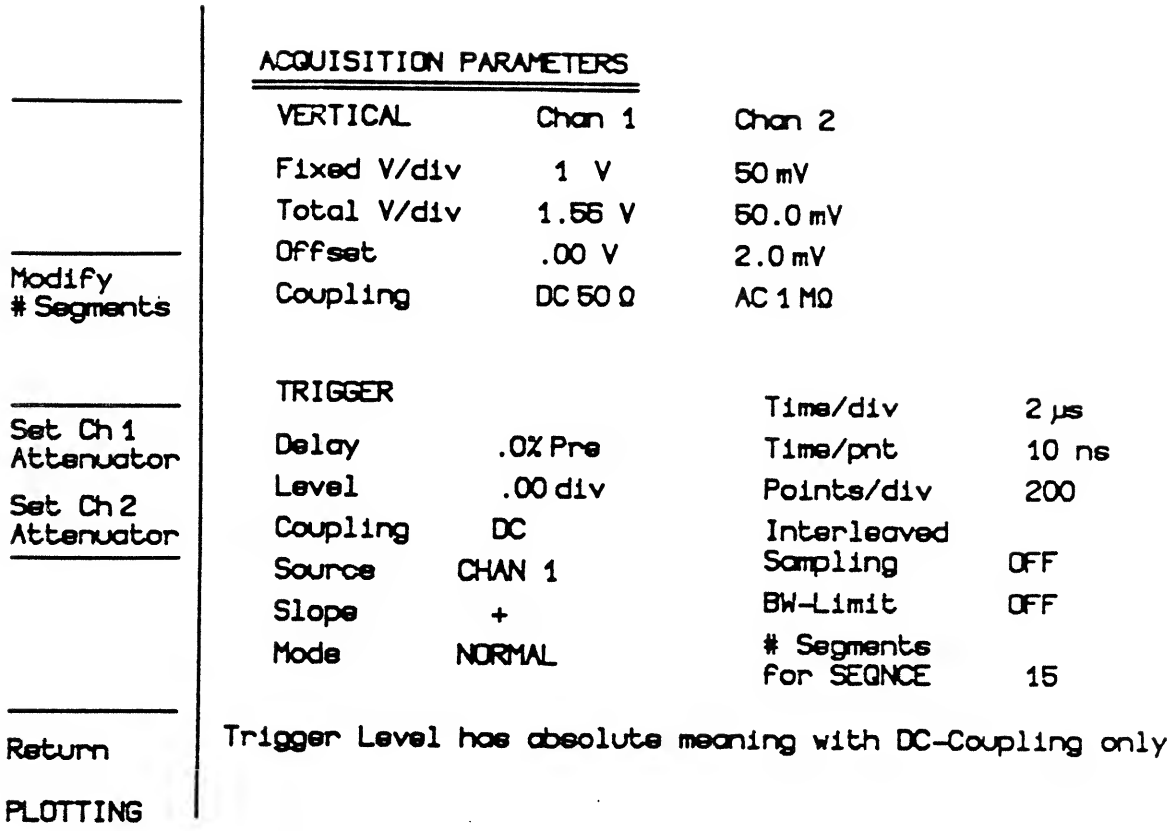
Remove top cover, locate the 9400-8.

- Set the scope to 50us/div, auto-trigger, RIS OFF
- Probe pin 2 or 3 with a calibrated high precision counter with a low Capacitance probe. You should measure 50 MHz +/- 1 khz.
- Set the scope to 20us/div, auto-trigger, you should measure 100 MHz +/- 2 kHz.

If the time base is bad the 100 Mhz crystal may be bad, or the 9400-4 TDC board is a fault.

Fig. 1 9400-8 CLK BUS





PANEL STATUS DISPLAY

Figure 6

7. Press the following sequence of buttons

   Return, Menu Off

8. Input the WWV signal to Channel 1.

9. Adjust the VERTICAL gain (Volt/div and VAR settings) to get a 6 division peak-to-peak signal.

10. Select the TRIGGER mode: SINGLE (HOLD).

11. Press DUAL GRID. A dual grid is displayed on the screen.

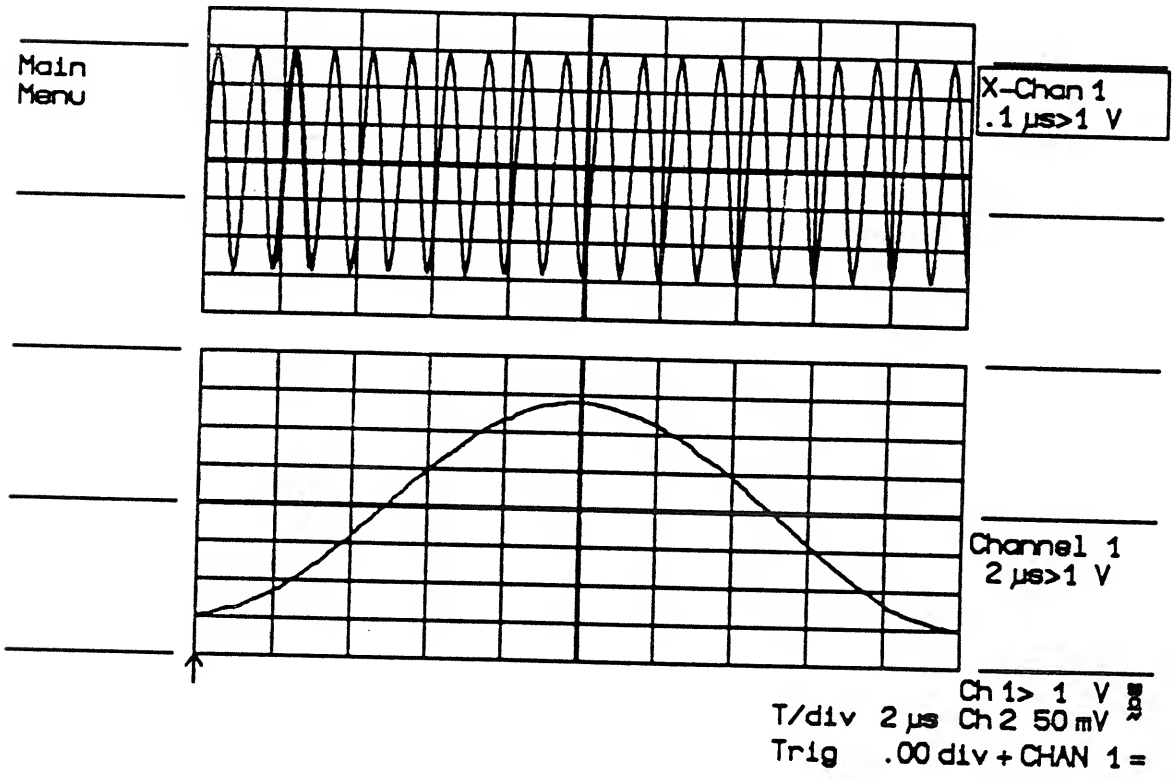
12. Press the following sequence of buttons:

    Press EXPAND A
    Press Display Control RESET
    REDEFINE Channel 1 (channel 1 is now the source trace).

13. Adjust the TIME MAGNIFIER to 0.1 µsec/div;

14. Turn the DISPLAY CONTROL Horizontal POSITION knob to select the 3rd period on the trace.

15. Using the Vertical POSITION knob put the expanded track on the second grid as shown in Figure 7.



WWV SIGNAL; FIRST EXPANSION

Figure 7

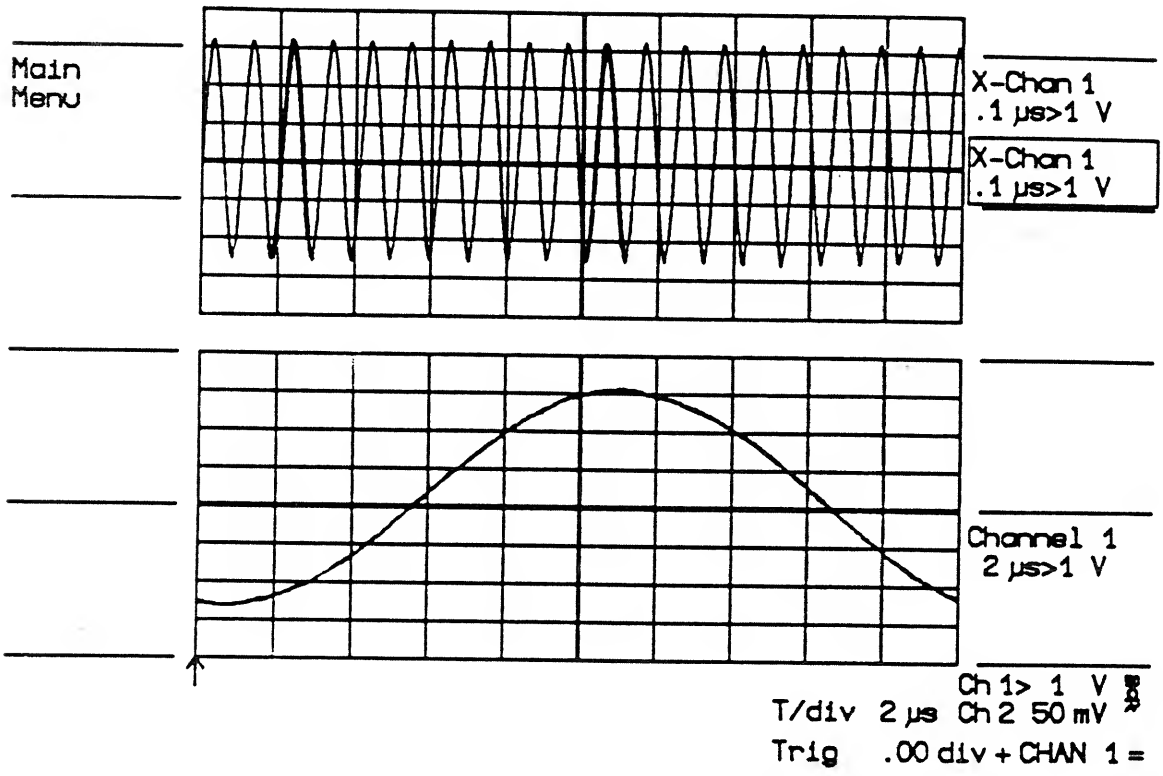
16. Press the following sequence of buttons:

    EXPAND B.
    DISPLAY CONTROL SELECT.
    REDEFINE Channel 1 (channel 1 is now the source trace).

17. Adjust the TIME MAGNIFIER to 0.1 µsec/div;

18. Turn the DISPLAY CONTROL Horizontal POSITION knob to select the 13th period.

19. Using the vertical and horizontal POSITION knobs, overlay the two expanded traces on the lower grid as shown in Figure 8.



WWV SIGNAL; SECOND EXPANSION

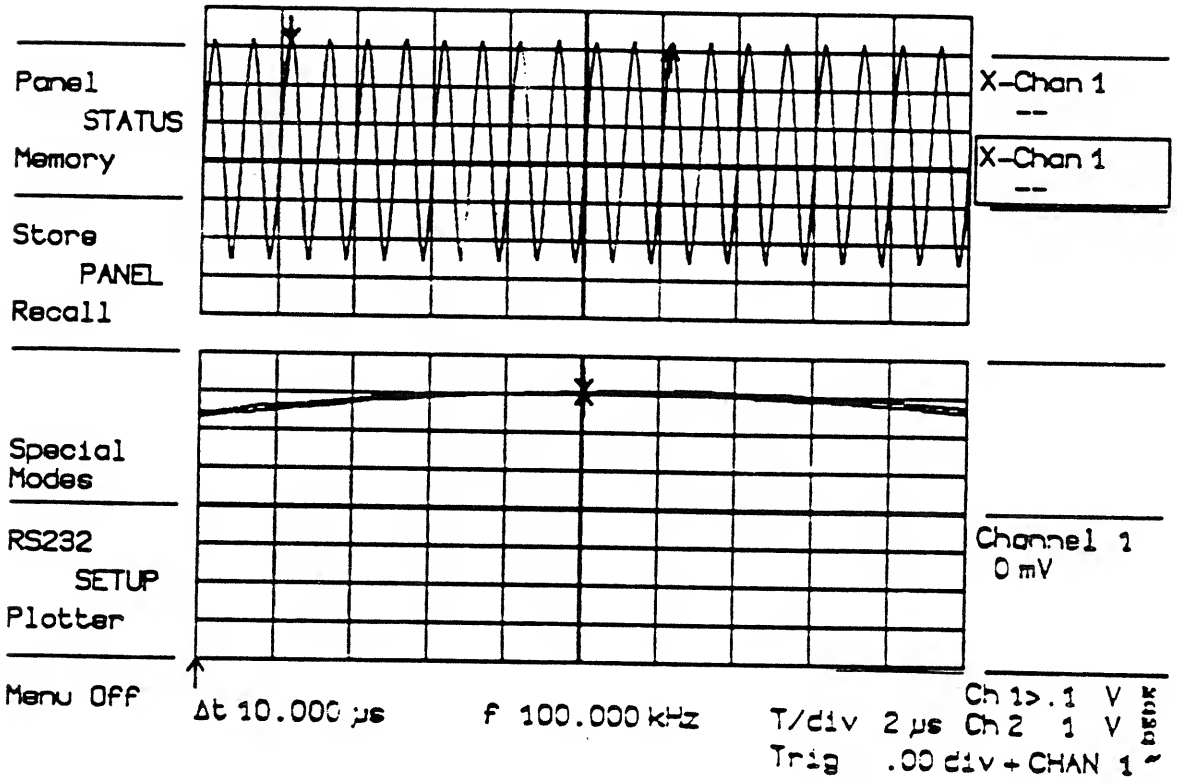
Figure 8

Measurement of the time difference (frequency)

20. Press the TIME cursor button.

21. Place the REFERENCE cursor on the 3rd period (control the cursor position on the upper grid).

22. Put the DIFFERENCE cursor (CURSOR POSITIONS) on the 13th period (control the cursor position on the upper grid) and adjust alignment of the two cursors with DIFFERENCE cursor (control the cursor position on the lower grid) as shown in Figure 9.



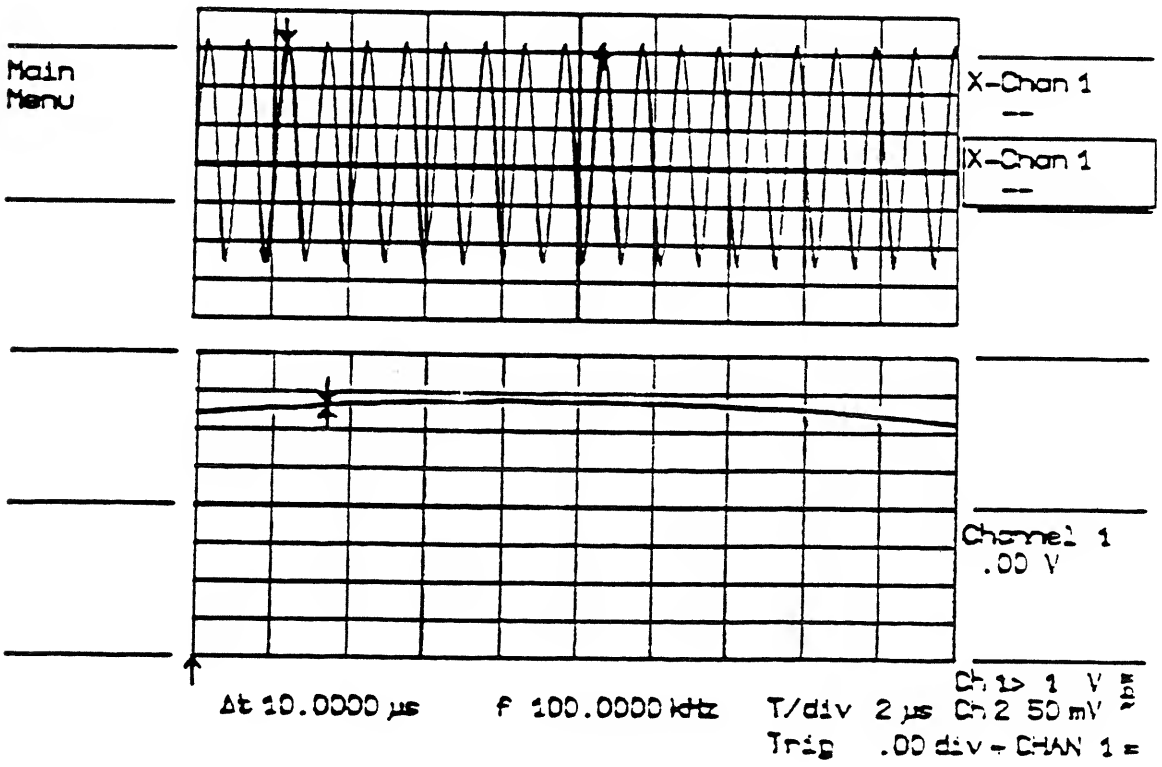
WWV SIGNAL: POSITION OF THE CURSORS

Figure 9

23. Press the following sequence of buttons:

    Main Menu
    Special Modes
    Mod. Common Expand (selects COMMON EXPANDED ON)
    Return
    Menu Off

24. Turn the TIME MAGNIFIER (DISPLAY CONTROL) to select the maximum expansion. Adjust the two cursors with the DIFFERENCE Cursor knob as shown in Figure 10.



WWV SIGNAL; MAXIMUM EXPANSION

Figure 10

25. The DIFFERENCE time reading must be in the interval 9.9996 µsec to 10.0004 µsec.

    Reading accuracy ± 400 psec (± 1 dot) on time reading.

2.2 Symptoms and Diagnosis

In this section some attempt is made to suggest possible problems which be the cause of observed symptoms in a defective 9400.

2.2.1 No Image on Screen

IF the **fan is still** AND **rear panel LEDs are off**

THEN check main power fuse on back panel, power plug, etc.,

ELSE IF the **fan runs** AND **rear panel LEDs are off**

THEN check low voltage supplies and their connections
check for ripple > 500 mV on any one of the low voltage DC power supplies

ELSE IF **rear LEDs are on** AND **front-panel LEDs are off**

THEN check power supplies to, and operation of, 9400-1 main board

ELSE IF **front-panel LEDs are on**

THEN check heater glow at rear of CRT
check 9400-7 correctly fitted at CRT base
check all cables 9400-2 and 9400-7 (4)

check fuses 9400-2
check that the thermo-switch is open on 9400-2 <1.2.5.1>
check RESET line high <1.2.5.1>
check signals on 9400-2 bus <1.2.2.1>
check amplifier inputs on 9400-2 <1.2.7.1>
check EHT generator on 9400-2 <1.1.9.1>
check sync signal from back panel
at J17 pin 13 9400-1 <1.1.8.1>

The fault is probably on the 9400-2 (1.2) or 9400-1 (1.1.16), but may be caused by no response from a peripheral of the 68000 - note that all boards are peripherals - which can be checked by looking at the re-boot circuit <1.1.2.1>.

2.2.2 Abnormal Image on Screen

IF	the **display is slightly out of focus**, but otherwise normal	
THEN	adjust focus control on 9400-7	(2.4.7)
OR	check function of 9400-7	(1.7)
	check HT supplies from 9400-2	(1.2.11)
ELSE	IF **display** dim but otherwise normal	
THEN	adjust brightness on 9400-7	(2.4.7)
OR	check function of 9400-7	(1.7)
	check HT supplies from 9400-2	(1.2.11)
	check luminance signal from 9400-2	(1.2.4)
	check potentiometers	(1.5.2)
	check potentiometer controls	(1.1.21.3)
ELSE	IF the **display is badly out of focus** or just a patch of light	
THEN	check function of 9400-7	(1.7)
	check HT supplies from 9400-2	(1.2.11)
ELSE IF	entire image has the **wrong width**	
THEN	adjust X amplifier gain	(2.4.2.3)
OR	check signal into X amp	(1.2.7+8)
ELSE IF	entire image has the **wrong height**	
THEN	adjust Y amplifier gain	(2.4.2.3)
OR	check signal into Y amp	(1.2.7+8)
ELSE IF	the entire image is **distorted in X**	
THEN	check X deflection processing	(1.2.6-8)
ELSE IF	the entire image is **distorted in Y**	
THEN	check Y deflection processing	(1.2.6-8)
ELSE IF	the entire image is **shifted sideways**	
THEN	adjust X offset	(2.4.2.2)
OR	check X circuits	(1.2.6-8)
OR	adjust centralizers	(2.4.7.4)
ELSE IF	the entire image is **shifted vertically**	
THEN	adjust Y offset	(2.4.2.2)
OR	check Y circuits	(1.2.6-8)
OR	adjust centralizers	(2.4.7.4)

ELSE IF the **lines do not join up** correctly

THEN adjust vector controls (2.4.2.5)
OR check circuits (1.2.4)
ELSE IF the grids/menus are good but the **waveforms bad**

THEN IF double arrows show **waveform 1 (2) is right off screen**
THEN check the input offset at socket with Hi-Z voltmeter (2.4.1.4)
AND check the input protection diodes (1.1.31.1)

ELSE IF **no waveforms** on Channel 1 (2)

THEN check the entire signal path from Channel 1 (2) input

ELSE IF **waveforms** on Channel 1 (2) **distorted**

THEN check 9400-3 Channel 1 (2) (1.3)

ELSE IF **bad waveforms** on both channels

THEN check 9400-8 is present <5.0.2>
check it has good signals CK, CKR, SYNC (1.4)
check 9400-4 (1.4)
check 9400-1 (1.1)

ELSE IF **no waveforms** on either channel

THEN check 9400-8 is correctly inserted (5.0.3)
check 9400-8 carries correct signals (1.8)
check 9400-4 functions (1.4)

2.2.3 Abnormal Control Responses

2.2.3.1 Potentiometer Problem

IF **only one is faulty**

THEN IF accessible from rear

THEN probe with scope/meter for levels at ends and slider

ELSE remove front panel and test

IF potentiometer seems good, probe multiplexer output C pin 8 on 9400-5 (1.5.2) for level change with rotation

IF **no signal** change DG508 or test its control signals (1.5.2)

ELSE (several or all do not work)

probe multiplexer output, C pin 8 on 9400-5 (1.5.2) or front-panel connector pin 9 on 9400-1 (AN0) (1.1.21.3) <5.1.1> to see response to rotation

check DG508 control signals

IF **DG508 signal absent or wrong** remove bottom cover (5.0.1) and check signals on 9400-5 cable <5.1.1> (1.1.21.3) FA1-3, etc.

IF necessary investigate front-panel control circuit (1.1.21)

2.2.3.2 Switch Control

IF **only one is switch bad**

THEN check switch with meter
OR investigate signals (1.5.3) (1.1.21.4)

ELSE **(several or all do not work)**

IF all the switches execute the wrong function

THEN check that the cable is correctly inserted between 9400-1 and 9400-5 at both ends

ELSE check power on 9400-5 investigate signals (1.5.3) or remove bottom cover (5.0.1) and probe 9400-5 connector <5.1.1> (1.1.21) probe front-panel controller (1.1.21)

2.3 Fault Finding on Individual Boards

This section includes suggestions for locating faults on individual boards of the 9400, in a somewhat anecdotal manner, as a comprehensive list could not be made.

2.3.2 Display Board

2.3.2.1 No Image on Screen

IF there is **no image** on the screen

THEN check the thermo-switch, which is the round component at the center of the MOSFET heat sink; it should be open circuit in a working DSO. <1.2.5.1>

IF it is closed

THEN there is over heating; check the amplifiers <1.2.8.1>

ELSE (it is open) check one pin is at -15 V and the other is between -1 V and +1 V.

IF (lower than -1 V OR higher than +1 V)

THEN check the RESET line (1.2.5), which should be TTL high. <1.2.5.1>

IF the RESET line is TTL low

THEN check the source (9400-1 J17/2)(1.1.3).

ELSE

IF -1 V > thermo-switch > -5 V

THEN check Q67 and 1N748 zener <1.2.5.1>

ELSE

IF -5 V > thermo-switch > -15 V

THEN check Q52 and Q41 <1.2.5.1>

ELSE

IF +15 V > thermo-switch > +1 V

THEN check Q51 and Q42 <1.2.5.1>

2.3.7 CRT Services Board

2.3.7.1 IF No Image is Present

THEN check voltages on 9400-7:

600 V	580 V
60 V	75 V
Z	-2 V
ZC	0 V

IF 60 V -> 20 V AND 600 V -> about 10 V

THEN connecting ZC to ground will overcome the protection system to aid investigation

WARNING

IF there is a point of light at the center of the screen you must power down OR remove the ZC override. If you want to continue, power down and disconnect the EHT cable, placing in a dummy load or safe insulating receptacle.

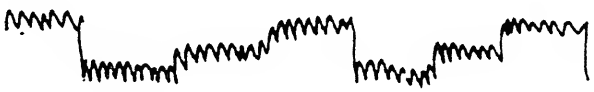
2.3.9 Power Supplies

2.3.9.1 Power Supply Noise Problem

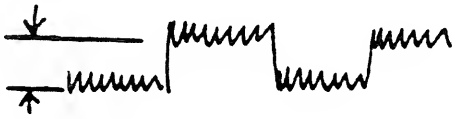
Some power supplies produce noise on the supply rail which can produce disturbance to the display of the 9400. The diagrams below show the maximum acceptable noise - any unit giving more than this should be replaced. The diagrams show what would be seen using a 9400 with a probe.

A Appearance. The noise looks like this:

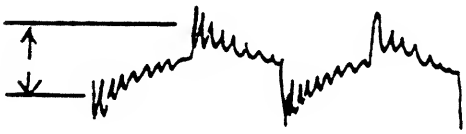
|<- 10 or 20 msec->|



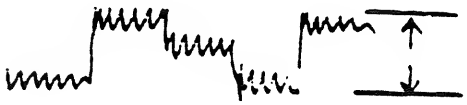
B Maximum low frequency ripple must be less than 30 mV p-p



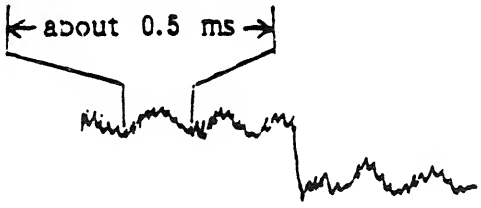
C Maximum high frequency ripple must be less than 30 mV p-p



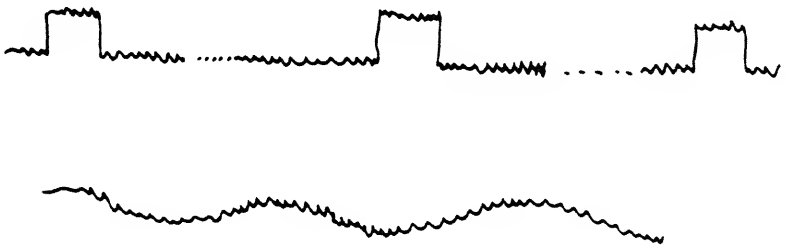
D Total ripple must be less than 50 mV p-p



E There must be no oscillations:



A similar problem is that some power supplies give sudden short changes in level. If this results in visible screen problems, reject the power supply. Any power supply which gives jumps of more than 50 mV should be rejected. The second, smooth variation is acceptable, because it causes no apparent trouble.



2.4 Adjustment Procedures for 9400

2.4.0 Introduction

This section describes all the adjustments which can be made in the field without the special LeCroy test gear which is only available at 9400 repair centers. Note that any adjustment which is omitted from this manual must not be touched, as maladjustment of certain presets can seriously degrade performance though this may not at first be apparent. Handling of boards should be done in such a way as to minimize the risk of moving a preset.

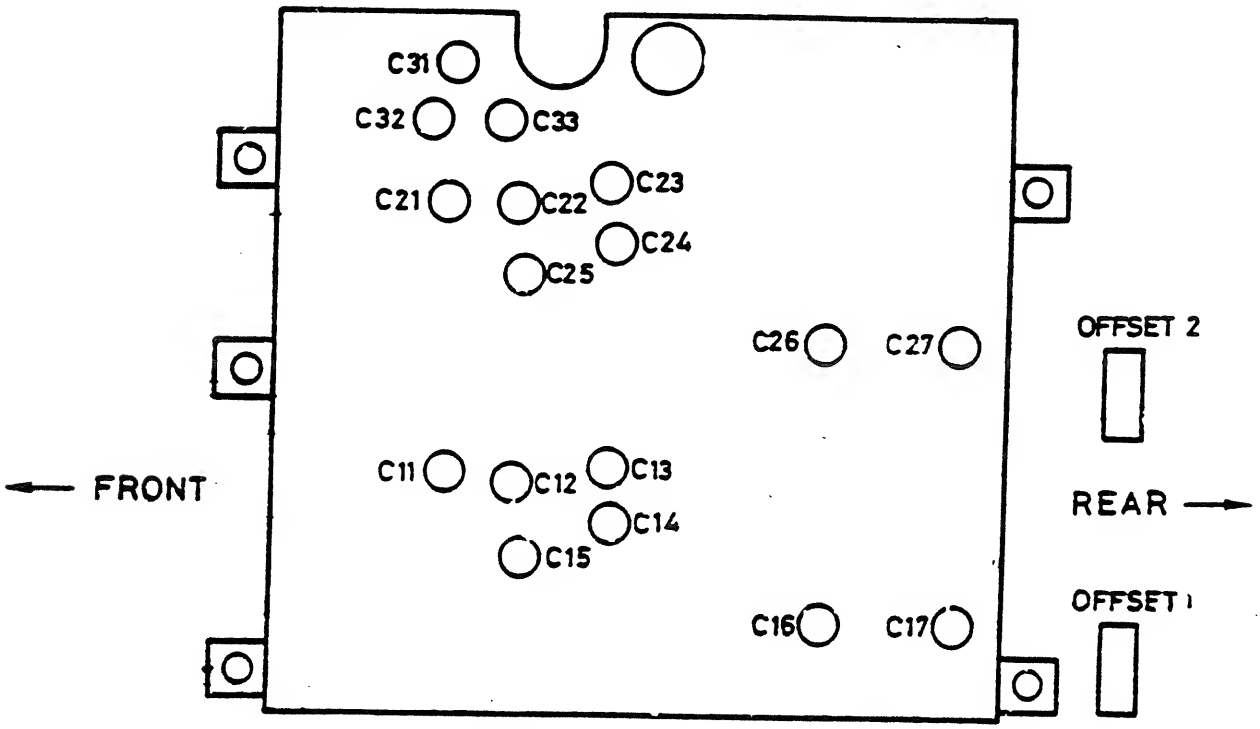
Some procedures require that the internal test software of the 9400 be set up; this is described in detail in paragraph 3.1.

The present adjustment procedures are contained in the computer assisted adjustment section of the 9400 calibration software package CALSOFT (CS01, CS02). It guides the service engineer through all the procedures and sets the 9400 up automatically as required for each individual adjustment. The present procedures are in compliance with the calibration limits applied in CALSOFT.

2.4.1 9400-1 Main Board

2.4.1.1 Introduction

The 9400-1 main board carries the front-end amplifiers, attenuators and trigger controls. There are numerous presets which can be adjusted in the field, for example after replacement of a HVV 200.



Presets on the 9400-1 front-ends

Figure 2.4.1.1

2.4.1.2 Power Supply

Check the supply voltages ± 15.01, ± 0.02 V, and ± 5.17 ± 0.01 V nominal on the 9400-9A board.

The ELBA supplies can be adjusted through the DSO rear panel.

2.4.1.3 Probe Calibrator

DSO probe calibrator set to 1 V.

Adjust potentiometer PO(F1) to 1 V at the probe calibrator output (within 0.5%) using a 4-digit voltmeter, and hit N to check again.

Probe calibrator set to 2 V. Check with a 4-digit voltmeter.

If not OK (within 0.5%), double error (e.g. 2.005 --> 2.010) by adjusting potentiometer P1(F1), and go back to check 1 V again.

2.4.1.4 Gain Curves and Offset

Gain curves

Put the DSO into the internal test menu with TRIG SOURCE LINE, MODE NORM.

Start the DSO internal test 'gain curves', BWL ON, 5 mV/div CH 1 and 2.

Check that the gain curves are at least 1/4 division above the gain = 1 line (left edge) on the left flat-top and that the curves decrease to at least 1/4 division below the gain = .4 line (center).

Check that the gain curve is smooth without steps or kinks.

If not OK, HVV200 of corresponding channel is probably bad!

Replace the 9400-1 board.

Repeat the test for BWL OFF and 10, 20 and 50 mV/div gain.

Offset

Put the DSO into the internal test menu with TRIG SOURCE LINE, MODE NORM.
Start the DSO internal test 'Offset vs Gain', BWL ON, 5 mV/div CH 1 and 2.

Check that the curves are rather horizontal (difference beginning-end of slope < 1 div) and that deviations from the center line stay within 1.5 divisions. If not OK, adjust potentiometers P3(D7)/P2(B7) to make the curves as flat as possible with deviations for BWL ON/OFF symmetric around the center line.

Repeat the test for 10, 20 and 50 mV/div gain.

2.4.1.5 Check Input Impedance

Channel 1 and 2

Check the input impedance for CH 1 and 2. The 1 MΩ DC and 50 Ω inputs for all gains should be 1 MΩ, and 51 Ω within 1%.

Trigger

Set the DSO to EXT TRIG SOURCE, COUPLING DC.
Check TRIG input impedance 1 MΩ (± 5%).

Set the DSO to TRIG SOURCE EXT/10, COUPLING DC.
Check TRIG input impedance 1 MΩ (± 5%).

2.4.1.6 Overload Protection

Set the DSO to CH 1 and 2 50 Ω.
Check that overload protection is activated within 15 to 25 seconds after applying > 7 V.

If not OK, adjust potentiometer slightly P4,P5 (G8).

Wait for at least 10 minutes between tests in order to allow settling to ambient temperature!

2.4.1.7 Trigger

Check Couplings

Set the DSO to TRIG SOURCE EXT, COUPLING DC.
Apply a 10 kHz square wave signal 4 V p-p to EXT.
Use the adjusted probe and look at pin 6 or 7 of MVL407 (B13).
You should see the same square wave.

Set the DSO to TRIG SOURCE EXT, COUPLING HFRej.
Apply a 10 kHz square wave signal 4 V p-p to EXT.
Use the adjusted probe and look at pin 6 or 7 of MVL407 (B13).
You should see slower fall/risetimes (integration).

Set the DSO to TRIG SOURCE EXT, COUPLING LFRej.
Apply a 10 kHz square wave signal 4 V p-p to EXT.
Use the adjusted probe and look at pin 6 or 7 of MVL407 (B13).
You should see spikes at the signal edges (differentiation).

Set the DSO to TRIG SOURCE EXT, COUPLING AC.
Apply a 15 Hz square wave signal 4 V p-p to EXT.
Use the adjusted probe and look at pin 6 or 7 of MVL407 (B13).
You should see spikes at the signal edges (differentiation).

Level DC

Check the ± 12 V regulators on 9400-1 (F10/11); they have to be matched within 50 mV for correct trigger level calibration.

Set the DSO to CH 1, 1 MΩ DC, 500 mV/div, TRIG: COUPLING DC, SLOPE POS, LEVEL 0 div.
Apply a 100 Hz sine waveform 4 V p-p to CH 1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.
If not OK, slightly adjust potentiometer P6(C/D12) and enforce AUTO-CALIBRATION and check again.

Set the DSO to CH 1, 1 MΩ DC, 500 mV/div, TRIG: COUPLING DC, SLOPE NEG, LEVEL 0 div.
Apply a 100 Hz sine signal 4 V p-p to CH 1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH 1, 1 MΩ DC, 500 mV/div, TRIG: COUPLING HFRej, SLOPE NEG, LEVEL 0 div.
Apply a 100 Hz sine signal 4 V p-p to CH 1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO set to CH 1, 1 MΩ DC 500 mV/div, TRIG: COUPLING HFRej, SLOPE POS, LEVEL 0 div.
Apply a 100 Hz sine signal 4 V p-p to CH 1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/DIV, TRIG: SOURCE CH2, SLOPE POS, LEVEL 0, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE CH2, SLOPE POS, LEVEL +3 div, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2.
Check that crossing at trigger point is at +3 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE CH2, SLOPE POS, LEVEL -3 div, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2.
Check that crossing at trigger point is at -3 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL 0, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2 over EXT.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 1 V/div, TRIG: SOURCE EXT/10, SLOPE POS, LEVEL 0, COUPLING DC.
Apply a 100 Hz sine signal 8 V p-p to CH 2 over EXT.
Check that crossing at trigger point is at 0 divisions within 3 minor divisions.
If not OK, adjust by adding resistor 1/8 W 6.8K to 30K between base of Q5 to -5 or +5 V (depending on sign of deviation) on solder side; check again.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL 0, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2 over EXT.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL +1.5 V, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2 over EXT.
Check that crossing at trigger point is at +1.5 volt within 1 minor division.

Set the DSO to CH2 DC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL -1.5 V, COUPLING DC.
Apply a 100 Hz sine signal 4 V p-p to CH 2 over EXT.
Check that crossing at trigger point is at -1.5 volt within 1 minor division.

Bandwidth AC

Set the DSO to EXT DC.
Apply a 10 kHz square wave, about 20 V amplitude through 50 Ω 20 dB attenuator, 50 Ω feed through, to EXT.
Use the adjusted probe and connect to the base of Q5 below the input cover plate (the channel you are looking at should be adjusted first!)
Adjust C32 for no under-/overshoot.

Set the DSO to EXT/10 DC.
Apply a 10 kHz square wave, 0 dB, 50 Ω feed through, to EXT.
Use the adjusted probe and connect to the base of Q5 below the input cover plate.
Adjust C31/33 for no under-/overshoot,
C31: long time scale,
C33: short time scale.
If you had to adjust C31 or C33, go to previous adjustment C32.

Set the DSO to CH1 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH1, SLOPE POS, LEVEL 0, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH1 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH1, SLOPE NEG, LEVEL 0, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH1 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH1, SLOPE NEG, LEVEL 0, COUPLING LFRej.
Apply a 1 MHz sine signal 4 V p-p to CH1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH1 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH1, SLOPE POS, LEVEL 0, COUPLING LFRej.
Apply a 1 MHz sine signal 4 V p-p to CH1.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH2, SLOPE POS, LEVEL 0, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH2.
Check that crossing at trigger point is at 0 divisions within 1 minor division.

Set the DSO to CH2 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH2, SLOPE POS, LEVEL +3 div, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH2.
Check that crossing at trigger point is at 3 divisions within 1 minor division.

Set the DSO to CH2 AC 1 MΩ, 500 mV/div, TRIG: SOURCE CH2, SLOPE POS, LEVEL -3 div, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH2.
Check that crossing at trigger point is at -3 divisions within 1 minor division.

Set the DSO to CH2 AC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL +1.5 V, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH2 through EXT.
Check that crossing at trigger point is at +1.5 V within 1 minor division.
If not OK, adjust level with C32 (if CH2 is not adjusted, go to CH2 50 Ω DC for the following checks, but make sure that the generator offset is 0!

Set the DSO to CH2 AC 1 MΩ, 500 mV/div, TRIG: SOURCE EXT, SLOPE POS, LEVEL -1.5 V, COUPLING AC.
Apply a 1 MHz sine signal 4 V p-p to CH2 through EXT.
Check that crossing at trigger point is at -1.5 V within 1 minor division.

Set the DSO to CH2 AC 1 MΩ, 1 V/div, TRIG: SOURCE EXT/10, SLOPE POS, LEVEL 0, COUPLING AC.
Apply a 1 MHz sine signal 8 V p-p to CH2 through EXT.
Check that crossing at trigger point is at 0 divisions within 3 minor divisions.

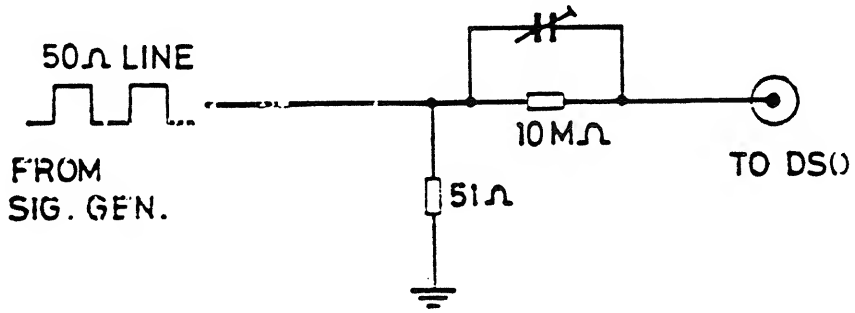
Set the DSO to CH2 AC 1 MΩ, 1 V/div, TRIG: SOURCE EXT/10, SLOPE POS, LEVEL +3 V, COUPLING AC.
Apply a 1 MHz sine signal 8 V p-p to CH2 through EXT.
Check that crossing at trigger point is at +3 V within 3 minor divisions.
If not OK, adjust level with C31/33 (if CH2 is not adjusted, go to CH2 50 Ω DC, but make sure that generator offset is 0!)
If you had to adjust, go back to previous C32 adjustment.

Set the DSO to CH2 AC 1 MΩ, 1 V/div, TRIG: SOURCE EXT/10, SLOPE POS, LEVEL -3 V, COUPLING AC.
Apply a 1 MHz sine signal 8 V p-p to CH2 through EXT.
Check that crossing at trigger point is at -3 V within 3 minor divisions.

2.4.1.8 Front-end

Channel 1

In the following adjustments the 4958 switch box is often used. It conveniently combines an adjusted /10 probe with attenuators. In the absence of a 4958, regular attenuators and a probe (like our Coline M12) which has been correctly compensated on an adjusted 9400 can be used. In the absence of a probe, an alternative test probe set up as shown in Figure 2.4.1.8 and properly adjusted on a good DSO, can be used.



Alternative Test Probe

Figure 2.4.1.8

Set the DSO to CH1, 1 V/div, 50 Ω, TRIG: SOURCE EXT, COUPLING DC, LEVEL 0.
Feed a 1 kHz square wave via switch box 4958 through EXT to CH 1.
Set BSD211/214 switch appropriately:
HVV200 no. XX XX 00 or 01 or 02 or 03: newer HVV with BSD214 transistor,
HVV200 no. XX XX /=00: older HVV with BSD211.
Set switch box 4958 to: 20 dB OFF, 20 dB OFF, 50 Ω OFF, Comp OFF.
Adjust signal amplitude to 6 divisions on screen.

Verify for the following settings that you always see the signal at 6 divisions:

CH 1		20 dB	20 dB	50 Ω	Comp	Reading
50 Ω,	1 V	OFF	OFF	OFF	OFF	6 div
50 Ω,	0.1 V	ON	OFF	OFF	OFF	6 div
50 Ω,	10 mV	ON	ON	OFF	OFF	6 div
1 MΩ,	10 mV	ON	ON	ON	OFF	6 div
1 MΩ,	0.1 V	ON	OFF	ON	OFF	6 div
1 MΩ,	1 V	OFF	OFF	ON	OFF	6 div
1 MΩ,	20 mV	ON	OFF	x	ON	6 div
1 MΩ,	200 mV	OFF	OFF	x	ON	6 div

Set the DSO to CH1 1 MΩ DC, 10 mV/div, TRIG: SOURCE CH1, COUPLING DC, LEVEL 0.
Apply a 10 kHz 6 V p-p square wave through 40 dB, 50 Ω feed through.
You should see 60 mV amplitude.

Set the DSO to CH1 1 MΩ DC, 100 mV/div, TRIG: SOURCE CH1, COUPLING DC, LEVEL 0.
Reduce attenuation to 20 dB.
Adjust C12 for no under/over-shoot.

Set the DSO to CH1 1 MΩ DC, 1 V/div, TRIG: SOURCE CH1, COUPLING DC, LEVEL 0.
Reduce attenuation to 0 dB.
Adjust C14/C13 for no under/over-shoot:
C14 long time-scale,
C13 short time-scale.

If you had to REadjust C14/C13, go back to adjustment C12.

Set the DSO to CH1 1 MΩ DC, 20 mV/div, TRIG: SOURCE CH1, COUPLING DC.
Apply a 1 kHz 6 V p-p square wave through switch box 4958 20 dB, Comp ON.

Adjust C11 for optimum risetime.

Set the DSO to CH1 200 mV/div, 1 MΩ DC, TRIG: SOURCE CH1, COUPLING DC, LEVEL 0.
Reduce attenuation to 0 dB.
Adjust C15 for optimum risetime.

Set the DSO to CH1 50 Ω DC, TRIG: SOURCE CH1, COUPLING DC.
Apply a 200 MHz sine signal with amplitude about 6 div to CH 1.
Adjust C17 for maximum amplitude.
Adjust C16 for maximum amplitude.
(Watch out for HVV oscillations at about 800 MHz!)

If you had to REadjust C16, go back to adjustment C17

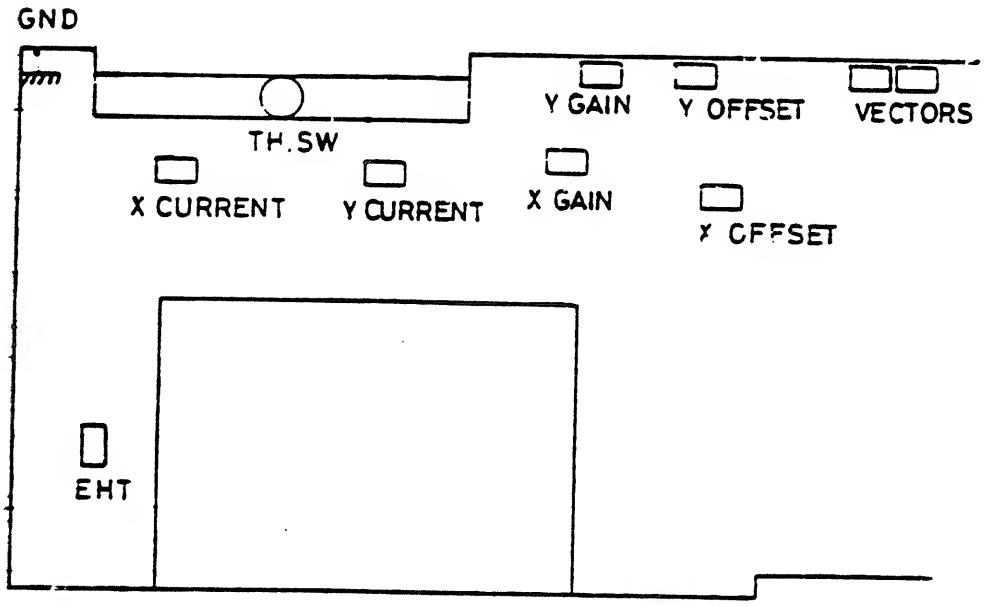
Channel 2

Repeat the above adjustment for channel 2. Add 10 to all capacitor labels, for example C11 becomes C21.

2.4.2 9400-2 and 9400-7 Display

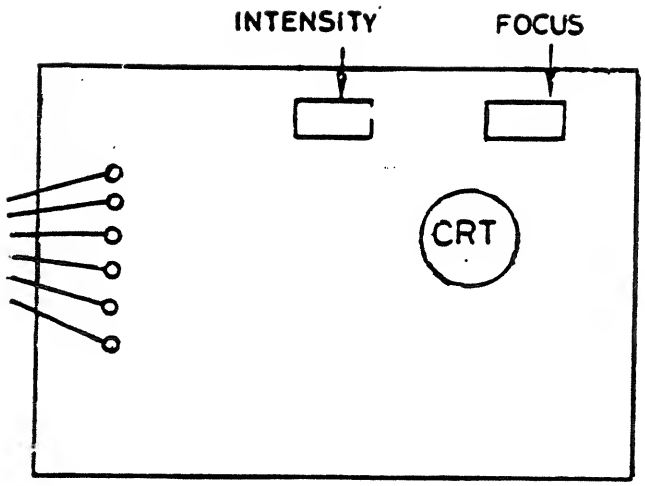
2.4.2.1 Introduction

The 9400-2 board carries a number of adjustments for the CRT image, many of which are field adjustable using procedures given below. The 9400-7 board carries much of the phosphor protection circuitry, and also the intensity and focus presets, which may be adjusted if there are no other contributory problems.



9400-2 Preset Controls

Figure 2.4.2.1



Intensity and Focus Controls

Figure 2.4.2.2

EHT

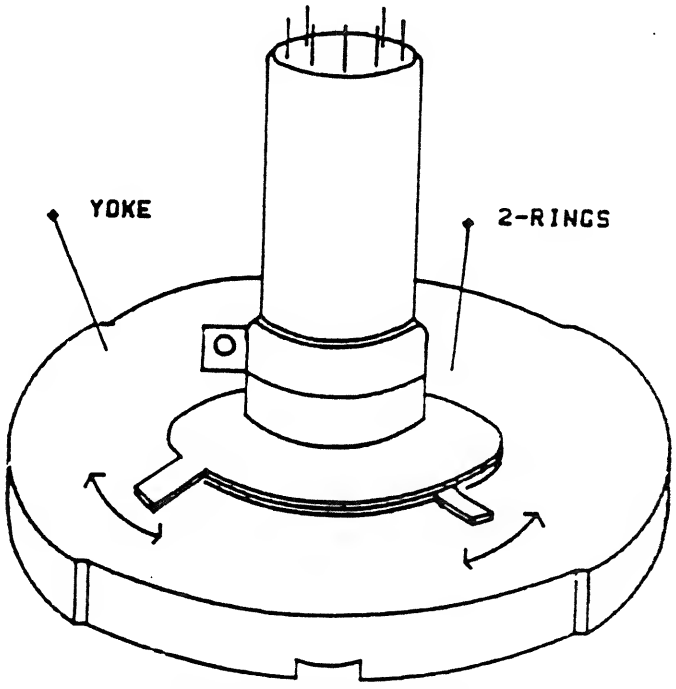
The 9400 should be set up to display a fairly complex image, and the two intensity controls on the front panel should be turned up; the EHT generator will then experience a substantial load. The EHT adjustment should be set to give an EHT potential of 11 kV. The 60 V and 600 V lines on the 9400-7 should also be checked.

Vector Joining

Adjust vectors with the help of the pair of vector potentiometers on the 9400-2 board right upper corner, above the connector.
Check that there are neither gaps nor overlaps in the letters T and S.

Centralizing Adjustment

If the X and Y amplifiers are correctly adjusted, and the image is poorly centered on the screen, it may be desirable to adjust the two magnetic rings on the yoke. This should not be done unless all other sources of image offset have been eliminated, and the amplifier offsets on the 9400-2 have been found to be correct.



Centralizing Rings

Figure 2.4.2.3

2.4.2.2 Adjustments

Image Position Adjustment

The offset controls may, in principle, be adjusted to obtain a centered image, provided that there are no other problems, see Centralizing Adjustment. Before making adjustments make sure that offsets at TP15 and TP21 are less than 10 mV for parts of the waveform after PGDIS and before SYDIS (1.1.16) (1.2.2), and other flat parts of the waveform between sections of vector drawing.

Intensity

Turn the DSO grid intensity off and the intensity to maximum.
Adjust the intensity potentiometer on the CRT board such that the center spot is just invisible.
If the intensity cannot be suitably controlled, then 9400-2 (1.2.4) (1.2.9) or 9400-7 (1.7) or 9400-1 (1.1.21.3) or the 9400-5 (1.5.2) must be checked.
This is the maximum allowed setting of the 9400-7 intensity control. It can be reduced if desired. Note that the yellow phosphor of the CRT in the 9400 is much more susceptible to damage by high beam currents than the usual blue/green phosphors.

Focus

Turn the grid intensity to maximum.
Adjust the focus control on the CRT board to optimize the image, taking into account all parts of the screen. If an expanded trace is selected, the selection box should be clearly separable from the menu separators.
If an adequate focus cannot be obtained, then the 9400-7 (1.7) or its power supplies on the 9400-2 (1.2.9) must be checked.

Image Size

Press the internal test button 'Calibration Constants' with border lines displayed.
Adjust the image size with the help of potentiometers GY/GX gain controls to the left of the two large yellow capacitors.

Yoke Rotation

Ensure that DSO power is OFF.
Rotate the image upright by turning the mechanical yoke position. For this loosen the screw on the yoke ring holder.

2.4.3 9400-3 ADC Board

2.4.3.1 Introduction

There are numerous preset controls on the 9400-3 ADC boards, which are set during manufacture. Only two of these are field-adjustable without the support of special LeCroy test gear. Every effort should be made to avoid disturbing these controls while handling the boards as they control the accuracy of waveform digitization. Note that the ADC boards may be interchanged for testing and fault finding, but they should always be replaced in their original position.

2.4.3.2 Gain Curves and Offsets

Gain curves

Put the DSO into the internal test menu with TRIG: source LINE, MODE NORM.
Start the DSO internal test 'Gain Curves', BWL ON, 5 mV/div CH 1 and 2.
Check that gain curves are at least 1/4 division above the gain = 1 line (left edge) on the left flat-top and that curves decrease to at least 1/4 division below the gain = 0.4 line (center).
Check that the gain curve is smooth without steps or kinks.
If not OK, the HVV200 of corresponding channel is probably bad!
Replace the 9400-1 board.

Repeat test for BWL OFF and 10, 20 and 50 mV/div gain.

Offset

Put the DSO into the internal test menu with TRIG: SOURCE LINE, MODE NORM.
Start the DSO internal test Offset vs Gain, BWL ON, 5 mV/div CH 1 and 2.
Check that the curves are rather horizontal (difference beginning-end of slope < 1 div) and deviations from the center line stay within 1.5 divisions.
If not OK, adjust potentiometers P3(D7)/P2(B7) to make the curves as flat as possible with deviations for BWL ON/OFF symmetric around the center line.

Repeat the test for 10, 20 and 50 mV/div gain.

2.4.3.3 Precision Adjustment for 1% Scopes

Adjust the DAC 800 (on the main 9400-1 board) offset to zero.
Measure voltage (mV) CAL1/CAL2 after LM324 (G6), in field G7 on one of the points where the two diodes are connected.
If larger than 1 mV, adjust potentiometer ZR (P8(J20) solder side) next to DAC 800, just behind -15 V power supply. It is difficult to access and a long slim screwdriver is needed.

Adjust the CH 1 and 2 HSH202 offset to zero.
Set the DSO to CH 1,2 50 Ω DC OFFSET 0, AUTO-CALIBRATE.
Measure voltage at CH 1,2 ADC SMB socket.
If larger than 3 mV, slightly adjust potentiometer P6 on the ADC board then enforce AUTO-CALIBRATION and check again (to do this, leave the ADC board in the DSO, put the GPIB board on the extender and reach in from the rear of the CRT!)

Put the DSO into the internal test menu with TRIG: SOURCE LINE, MODE NORM.
Start the DSO internal test Offset vs Gain, BWL ON, 5 mV/div CH 1 and 2.
Check that the curves are rather horizontal (difference beginning-end of slope < 1 div) and deviations from the center line stay within 1.5 divisions.
If not OK, adjust potentiometers P3(D7)/P2(B7) to make curves as flat as possible with deviations for BWL ON/OFF symmetric around the center line.

Repeat the test for 10, 20 and 50 mV/div gain.

2.4.3.4 Over-shoot

Channel 1

Set the DSO to CH 1, 50 Ω DC, 200 mV/div, TRIG: SOURCE: CH 1, COUPLING DC, Level 0.
Make sure that the CH 1 front-end is properly adjusted!
Apply a square wave with a risetime faster than 1 nsec (for example TEK PG502) through a 20 dB attenuator.
Adjust the step amplitude to 5 divisions.
Use the attenuator at input to attenuate possible reflections.
Adjust the capacitor between pins 8-10 of HSH202 such that signal overshoot is 1 minor division.
The signal should settle within 40 nsec.

Channel 2

Set the DSO to CH 2, 50 Ω DC, 200 mV/div, TRIG: SOURCE: CH 2, COUPLING: DC, LEVEL 0.
Make sure that the CH 2 front-end is properly adjusted!
Apply a square wave with a risetime faster than 1 nsec (for example TEK PG502) through 20 dB attenuator.
Adjust the step amplitude to 5 divisions.
Use the attenuator at input to attenuate possible reflections.
Adjust the capacitor between pins 8-10 of HSH202 such that signal overshoot is 1 minor division.
The signal should settle within 40 nsec.

2.4.4 9400-4 TDC Board

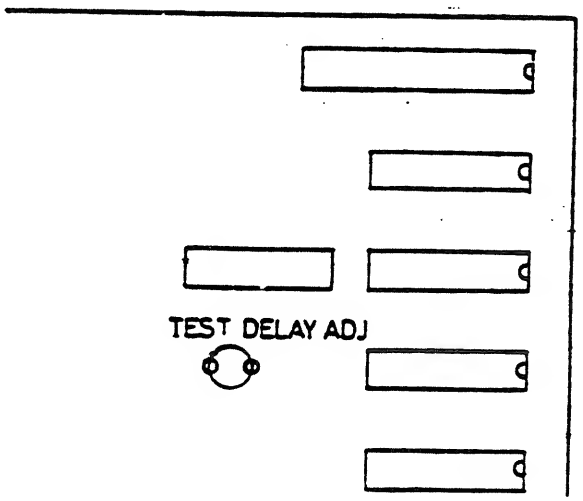
2.4.4.1 Frequency

Check the frequency (100 or 50 MHz) on the 2^{nd} or 3^{rd} line (from front) of the clock bus board.
If not OK, something basic is wrong with the TDC board.

Set the DSO to CH 1, 100 mV/div, 50 Ω DC, TRIG: SOURCE CH1, COUPLING AC, LEVEL 0, DELAY 19.99 msec post-trigger.
Apply to CH1 a sine wave of 100 kHz from a precision (better than 1 ppm) generator.
Adjust the 100 MHz ADJ such that the signal crosses the center point.
Turn the power off/on several times and check that the frequency is still OK. (This is to check that not too much adjustment was applied which may leave the oscillator locked out of the characteristic 100 MHz. If this happens, replace the crystal.)

2.4.4.2 Internal Trigger Delay

Set the DSO internal test 'TDC Calibration'.
Check (after a warm-up of at least 20 minutes) that there are two peaks of about the same width.
If not, adjust at TST DLY and check again.
It is very hard to reach this preset with a tool, but some help may be given using a probe adjustment screwdriver bent by 90 degrees. Also note that on ADC boards manufactured since February 1988 this varicap points upwards and is therefore easy to reach.



TDC Preset Control

Figure 2.4.4.1

2.4.5 Front-panel Board

2.4.5.1 LED Matching

All front-panel LEDs should be matched for color, in one of three grades (1.5.5). If urgent replacement of an LED is required, and the correct color match is not available, it is permissible to mismatch by one grade only in the case of a single LED, far from the others. For example, if one of a group fails, it can be replaced by one taken from a distant place on the panel, and the distant one can be replaced by the poorly matching one. Although the colors are fairly close, they look very bad when mixed.

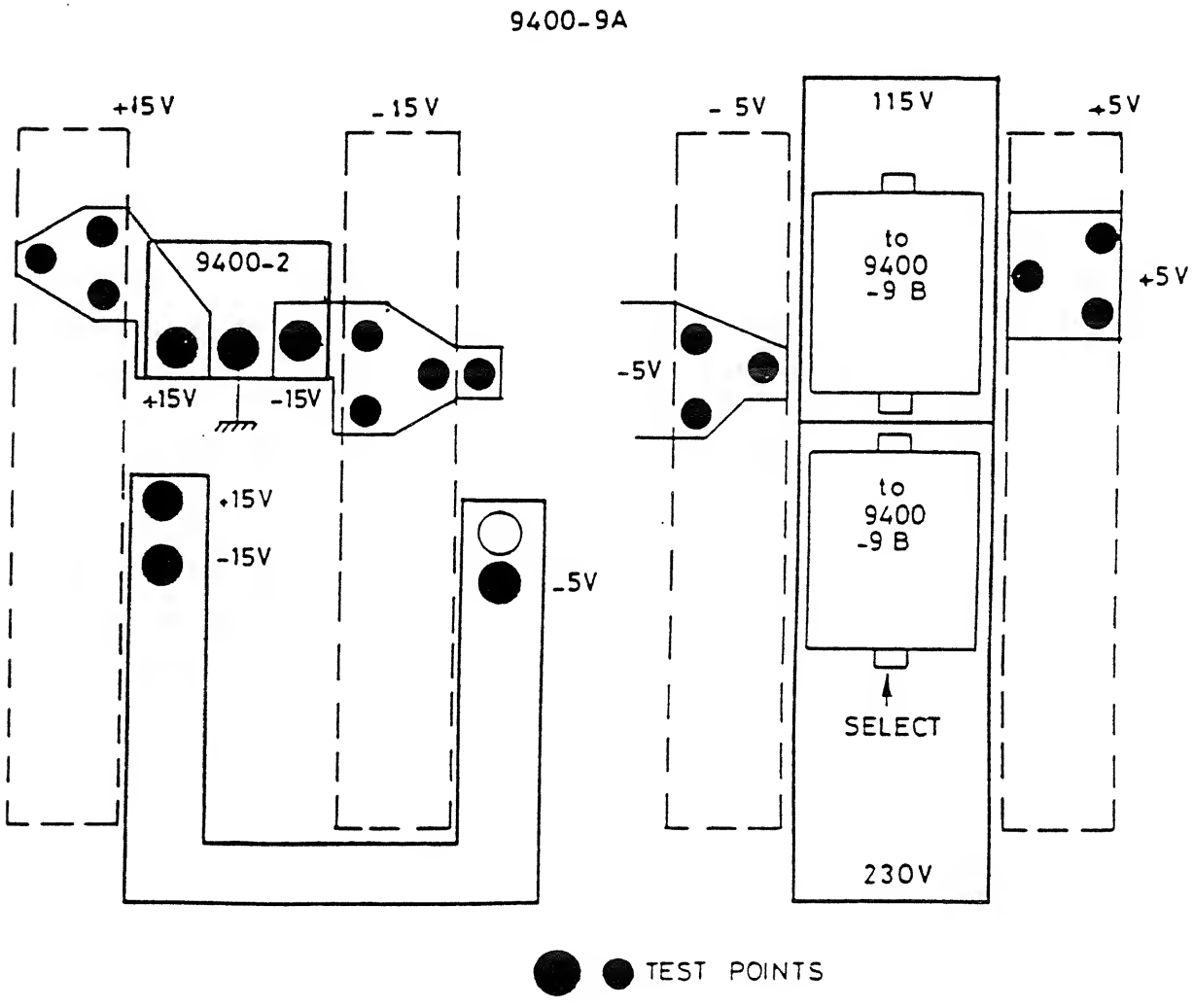
2.4.6 Changing the Input Line Voltage (Board 9400-9)

This will only be necessary when a 9400 has been transported, involving a change of local voltage.

Note that there are two operations, which must BOTH be done.

1. Ease out the little cover over the voltage adjuster <1.9.2> and take out the rotor. Rotate until the new voltage faces forward. Replace the rotor and the cover.

2. Remove the top cover (5.0.1) and move the large brown 12 pin plug on the 9400-9A <5.0.3> <2.4.9.1> to the 115 V or the 230 V position as appropriate. Check both settings carefully before powering up the DSO.



SETTING THE 115 V/220 V CONNECTION

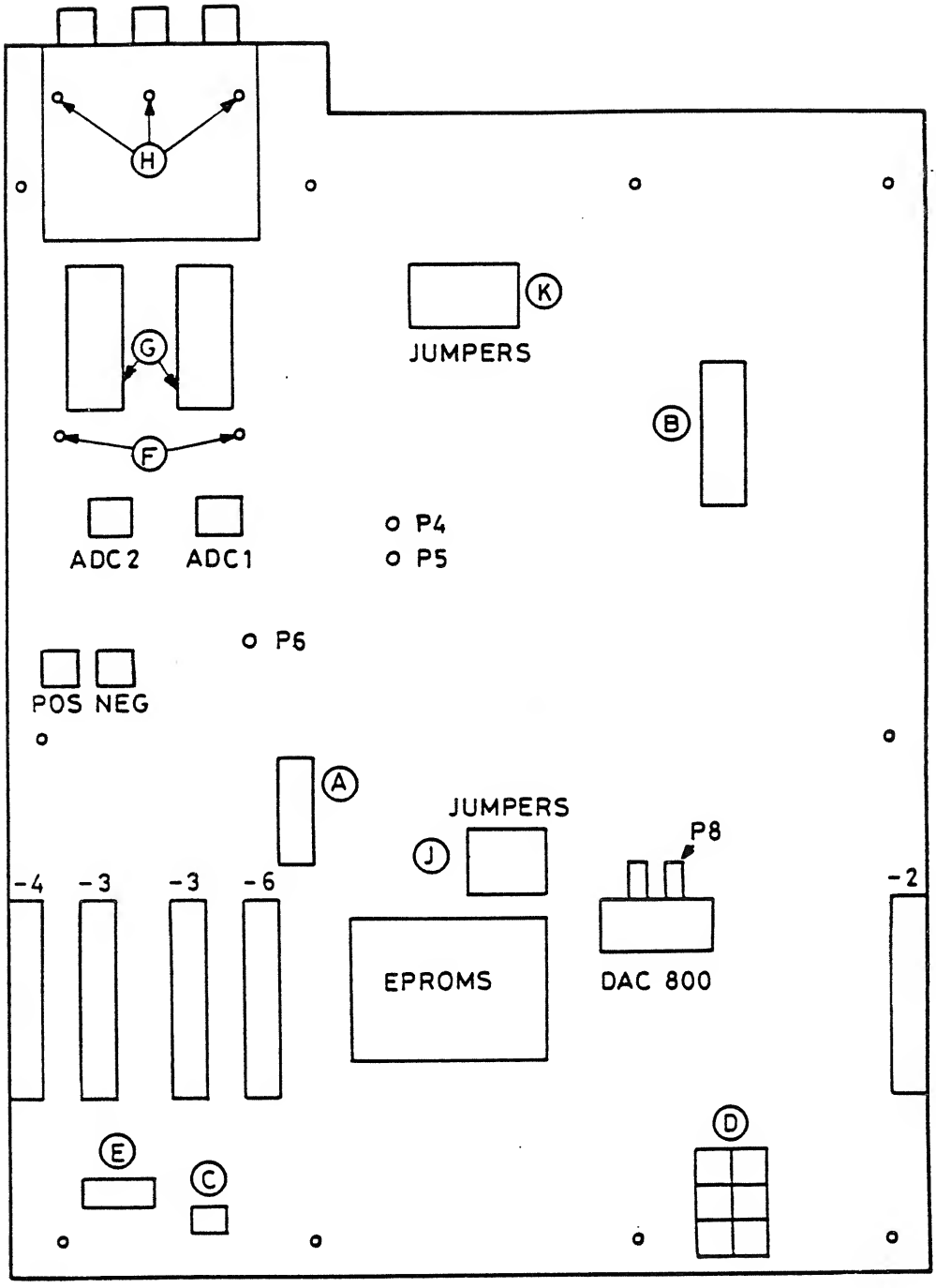
Figure 2.4.6

2.4.7 Potentiometers Cross Reference for the 9400-1 Board

Potentiometer	Used for	Name on Schematics	Location on board (Rev. F and up)
P0	Probe Calibrator	P0	F1 solder
P1	"	P1	F1 solder
P2	HVV200 Offset	no name	B7 solder
P3	"	no name	D7 solder
P4	Overload Protection	no name	G8 component
P5	"	no name	G8 component
P6	Trigger Level	P4	C/D12 comp
P8	Offset DAC 800	P6	J20 component

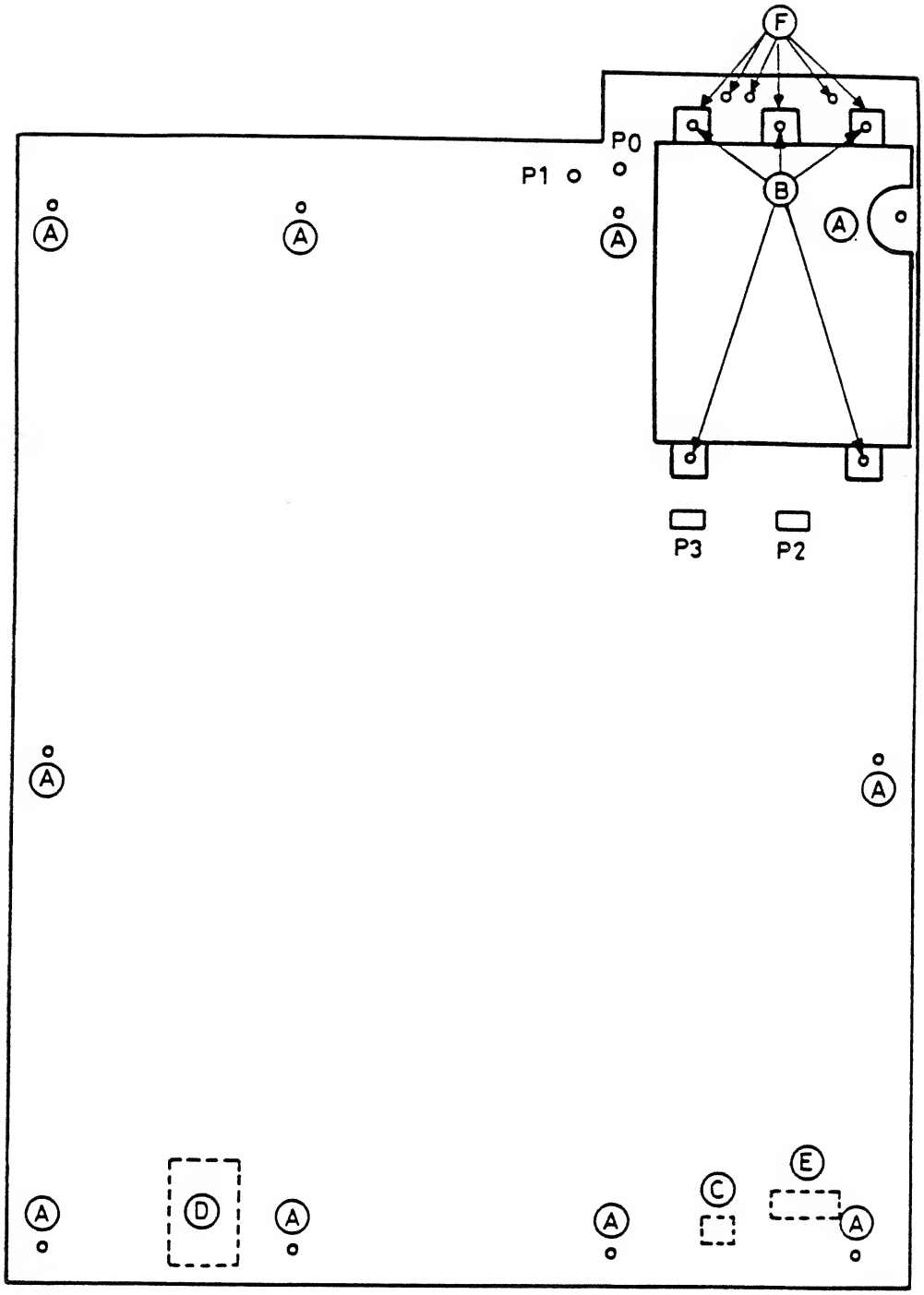
For Earlier Revisions

Revisions BC	remove resistor and place potentiometer P1 (2.2 MΩ)
All revisions	P0 on solder side
F and above	P2/P3 solder side
up to rev D	P0 component side between probe connectors



Top view of 9400-1 Main Board

Figure 2.4.7.1



Underside of the 9400-1 Main Board

Figure 2.4.7.2